Schematics Only for RK3588 NVR

RK_NVR_DEMO1_RK3588_LP4XD200P232SD8_V21

Main Functions Introduction

1) PMIC: RK806-1+DiscretePower
2) RAM: 2 x LPDDR4x 32bit(Option 2 x LPDDR4 32bit)
3) ROM: eMMC5.1(Option SPI Nand Falsh)
4) Support: 1 x TypeC(With DP TX)
5) Support: 1 x USB3.0 HOST + 2 x USB2.0 HOST
6) Support: 10 x SATA3.0 Connector (7pin)
7) Support: 1 x 4Lanes PCIe Connector
8) Support: 2 x HDMI2.1 TX + 1 x HDMI2.0 TX + 1 x HDMI1.4 TX
9) Support: 2 x 4Lanes MIPI CSI RX Camera Connector
10) Support: 2 x 10/100/1000 Ethernet(RGMII)
11) Support: 1 x Line Out, 1 x Line In
12) Support: 1 x Buzzer
13) Support: 1 x IR Receiver
14) Support: 1 x Power LED,1 x Ethernet LED,1 x HDD LED
15) Support: 1 x Recovery Key,1x Reset Key
16) Support: 1 x RS232
17) Support: 1 x RS485
18) Support: 1 x UART
19) Support: Debug UART(USB to UART),Debug JTAG (4Pin)

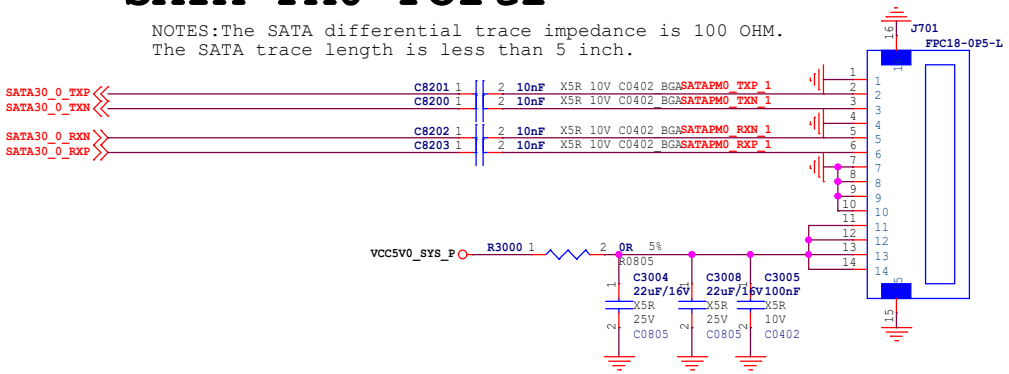
Note:

The RK806 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	00.Cover Page				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	1 of 43

SATA PM0 Port1

NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.



ShenZhen HugSun Technology Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	82. SATA3.0		
Date:	Friday, August 12, 2022	Rev:	V1.0
Designed by:	Wang	Sheet:	1 of 99

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

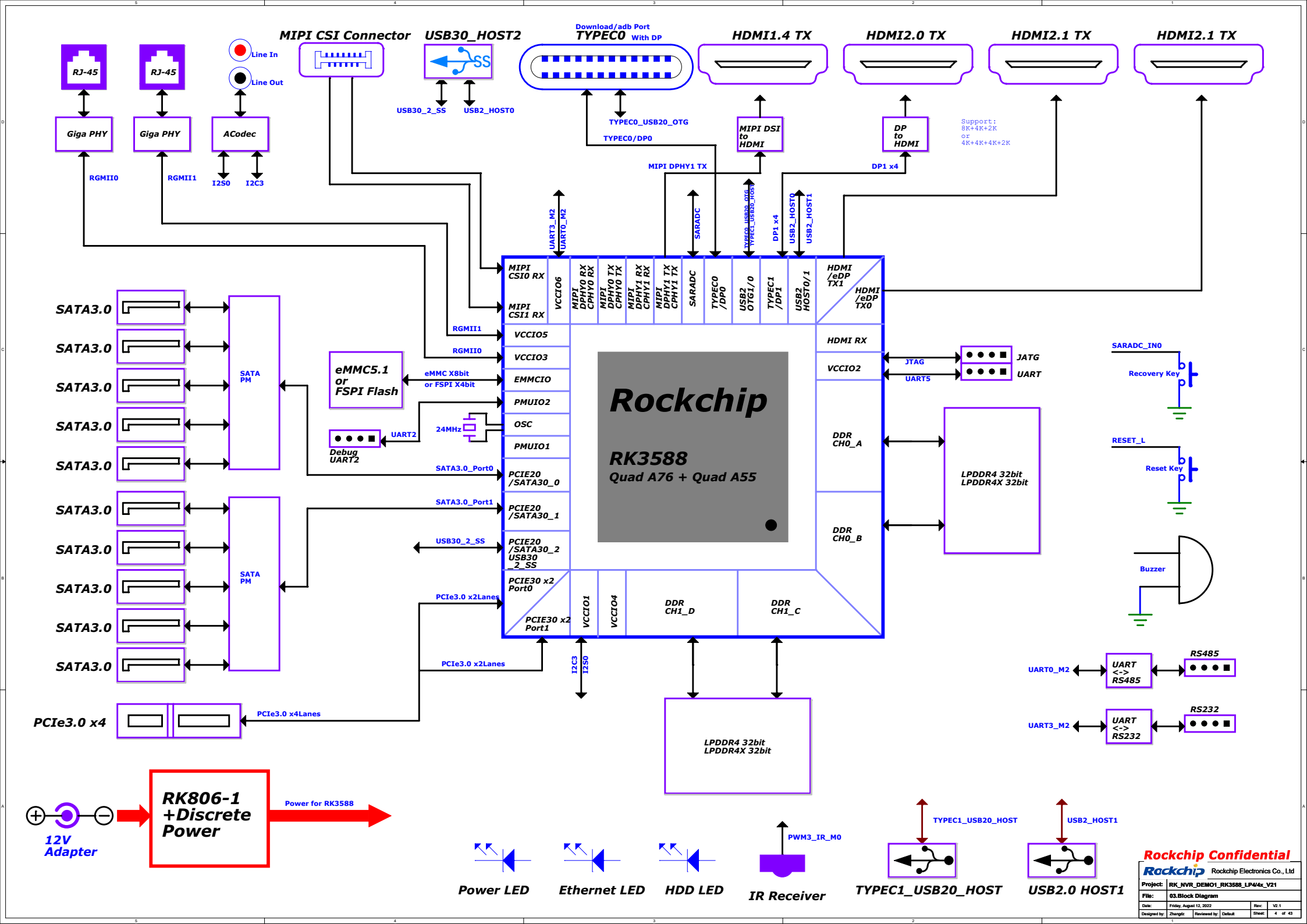
NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	01.Index and Notes				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	2 of 43

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-09-24	Zhangdz	1:Revision preliminary version	
V2.0	2021-12-08	Zhangdz	1:Invalid version	
V2.1	2021-12-28	Zhangdz	1:Change content Please Refer to: RK_NVR_DEMO1_RK3588_LP4XD200P232SD8_V21_20211228_Modify_Notes_CN	


MIPI CSI Connector
USB30_HOST2
Download/adb Port
TYPEC0 With DP
HDMI1.4 TX
HDMI2.0 TX
HDMI2.1 TX
HDMI2.1 TX
RJ-45
RJ-45
Line In
Line Out
Giga PHY
Giga PHY
ACodec
RGMII0
RGMII1
I2S0
I2C3
USB30_2_SS
USB2_HOST0
TYPEC0_USB20_OTG
TYPEC0/DP0
MIPI DSI to HDMI
DP to HDMI
DP1 x4
MIPI DPHY1 TX
Support:
8K+4K+2K
or
4K+4K+4K+2K
UART3_M2
UART0_M2
SARADC
TYPEC0_USB20_OTG
TYPEC1_USB20_HOST
DP1 x4
USB2_HOST0
USB2_HOST1
MIPI CSI0 RX
MIPI CSI1 RX
VCCIO6
MIPI DPHY0 RX CPHY0 RX
MIPI DPHY0 TX CPHY0 TX
MIPI DPHY1 RX CPHY1 RX
MIPI DPHY1 TX CPHY1 TX
SARADC
TYPEC0 /DP0
USB2 OTG1/0
TYPEC1 /DP1
USB2 HOST0/1
HDMI /eDP TX1
HDMI /eDP TX0
VCCIO5
VCCIO3
EMMC1O
PMUIO2
OSC
PMUIO1
PCIE20 /SATA30_0
PCIE20 /SATA30_1
PCIE20 /SATA30_2 USB30 _2_SS
PCIE30 x2 Port0
PCIE30 x2 Port1
VCCIO1
VCCIO4
DDR CH1_D
DDR CH1_C
HDMI RX
VCCIO2
DDR CH0_A
DDR CH0_B
Rockchip
RK3588
Quad A76 + Quad A55
SATA3.0
SATA3.0
SATA3.0
SATA3.0
SATA3.0
SATA3.0
SATA3.0
SATA3.0
SATA3.0
SATA3.0
SATA PM
SATA PM
RGMII1
RGMII0
eMMC5.1 or FSPI Flash
eMMC X8bit or FSPI X4bit
UART2
Debug UART2
24MHz
SATA3.0_Port0
SATA3.0_Port1
USB30_2_SS
PCIe3.0 x2Lanes
PCIe3.0 x2Lanes
PCIe3.0 x4
PCIe3.0 x4Lanes
I2C3
I2S0
JTAG
UART5
JATG
UART
LPDDR4 32bit LPDDR4X 32bit
LPDDR4 32bit LPDDR4X 32bit
SARADC_IN0
Recovery Key
RESET_L
Reset Key
Buzzer
UART0_M2
UART <-> RS485
RS485
UART3_M2
UART <-> RS232
RS232
12V Adapter
RK806-1 +Discrete Power
Power for RK3588
Power LED
Ethernet LED
HDD LED
PWM3_IR_M0
IR Receiver
TYPEC1_USB20_HOST
USB2_HOST1
TYPEC1_USB20_HOST
USB2.0 HOST1
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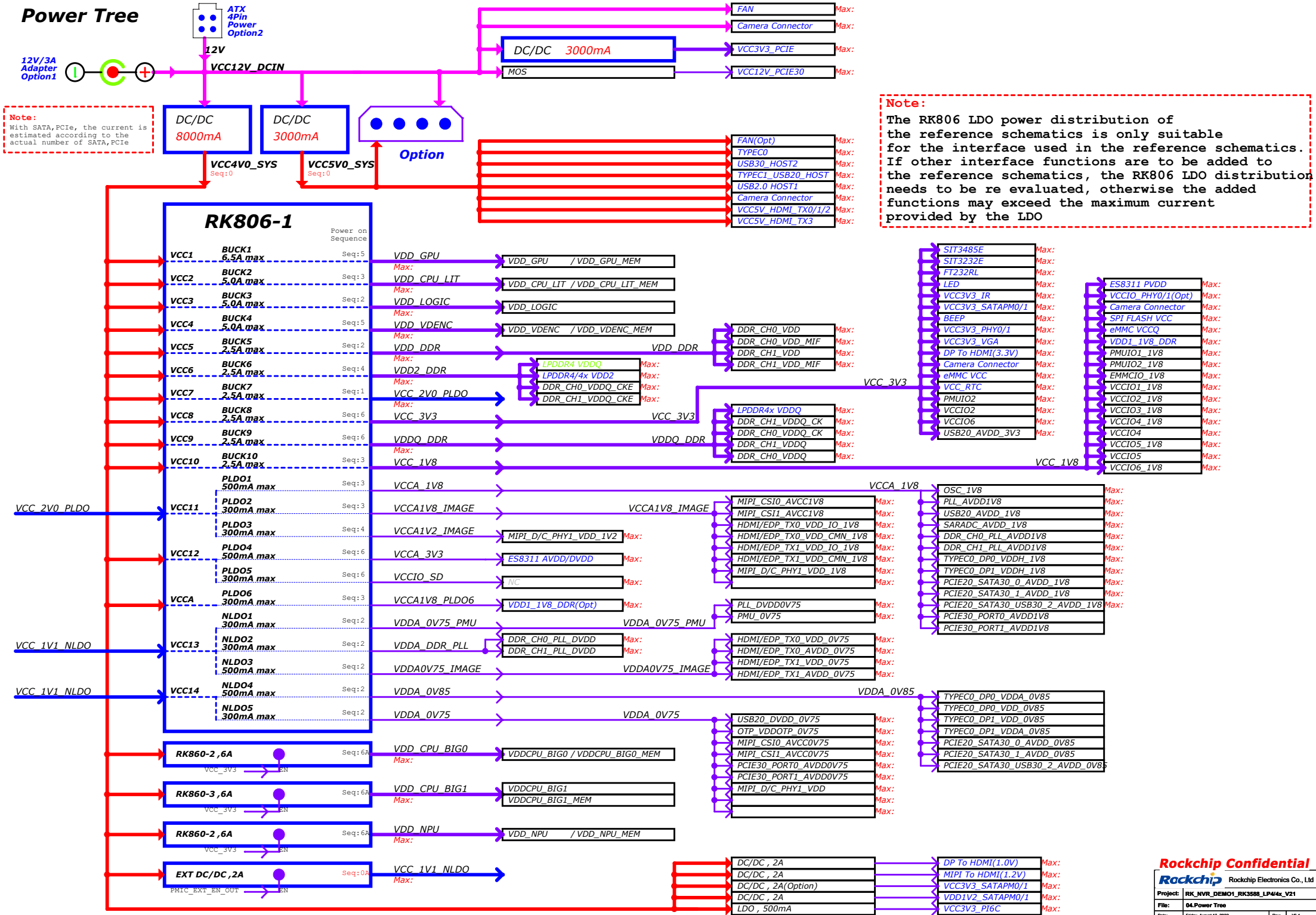
Rockchip Electronics Co., Ltd
Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21
File: 03.Block Diagram
Date: Friday, August 12, 2022
Rev: V2.1
Designed by: Zhangtz
Reviewed by: Default
Sheet: 4 of 43

Power Tree



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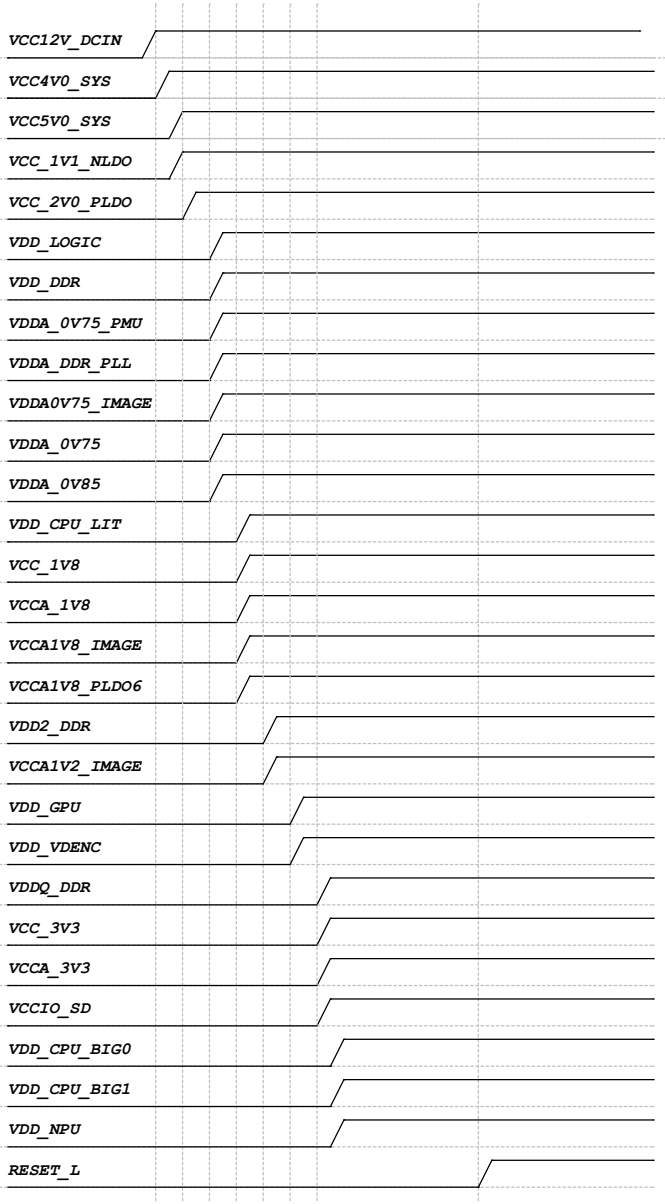
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	04.Power Tree
Date:	Friday, August 12, 2022
Rev:	V2.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	5 of 43

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC4V0_SYS	RK806_BUCK1	6.5A	VDD_GPU	Slot:5	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK2	5A	VDD_CPU_LIT	Slot:3	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK3	5A	VDD_LOGIC	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC4V0_SYS	RK806_BUCK4	5A	VDD_VDENC	Slot:5	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK5	2.5A	VDD_DDR	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK6	2.5A	VDD2_DDR	Slot:4	ADJ FB=0.5V	ON	1.1V LPDDR4/4x	TBD	TBD
VCC4V0_SYS	RK806_BUCK7	2.5A	VCC_2V0_PLDO	Slot:1	2.0V	ON	2.0V	TBD	TBD
VCC4V0_SYS	RK806_BUCK8	2.5A	VCC_3V3	Slot:6	3.3V	ON	3.3V	TBD	TBD
VCC4V0_SYS	RK806_BUCK9	2.5A	VDDQ_DDR	Slot:6	ADJ FB=0.5V	ON	0.6V LPDDR4/4x	TBD	TBD
VCC4V0_SYS	RK806_BUCK10	2.5A	VCC_1V8	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_IMAGE	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VCCA1V2_IMAGE	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC4V0_SYS	RK806_PLDO4	0.5A	VCCA_3V3	Slot:6	3.3V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD	Slot:6	3.3V	ON	3.3V	TBD	TBD
VCC4V0_SYS	RK806_PLDO6	0.3A	VCCA1V8_PLDO6	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDDA_0V75_PMU	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_IMAGE	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC12V_DCIN	EXT BUCK	8A	VCC4V0_SYS	Slot:0	4.0V	ON	4.0V	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO	Slot:0A	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_SYS	Slot:0A	5.2V	ON	5.2V	TBD	TBD
VCC4V0_SYS	RK860-2	6A	VDD_CPU_BIG0	Slot:6A	0.8V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK860-3	6A	VDD_CPU_BIG1	Slot:6A	0.8V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK860-2	6A	VDD_NPU	Slot:6A	0.8V	ON	DVFS	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8 VCC_3V3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8	1.8V
VCCIO1	Pin G20	1.8V Only	VDDIO1_1V8	VCC_1V8	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VDDIO2_1V8 VCCIO2	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin Y26	1.8V Only	VDDIO3_1V8	VCC_1V8	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VDDIO4_1V8 VCCIO4	VCC_1V8 VCC_1V8	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VDDIO5_1V8 VCCIO5	VCC_1V8 VCC_3V3	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VDDIO6_1V8 VCCIO6	VCC_1V8 VCC_3V3	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

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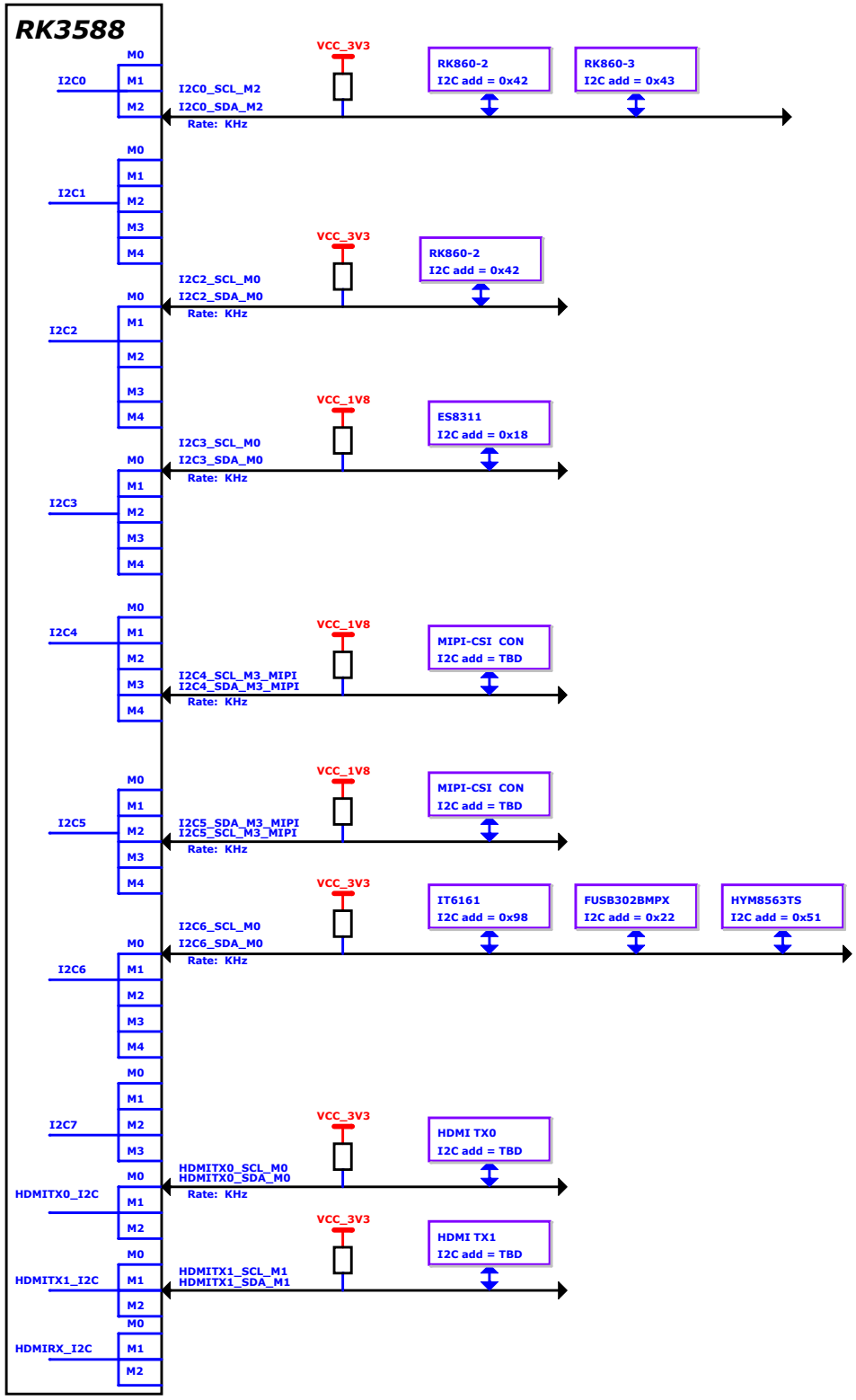
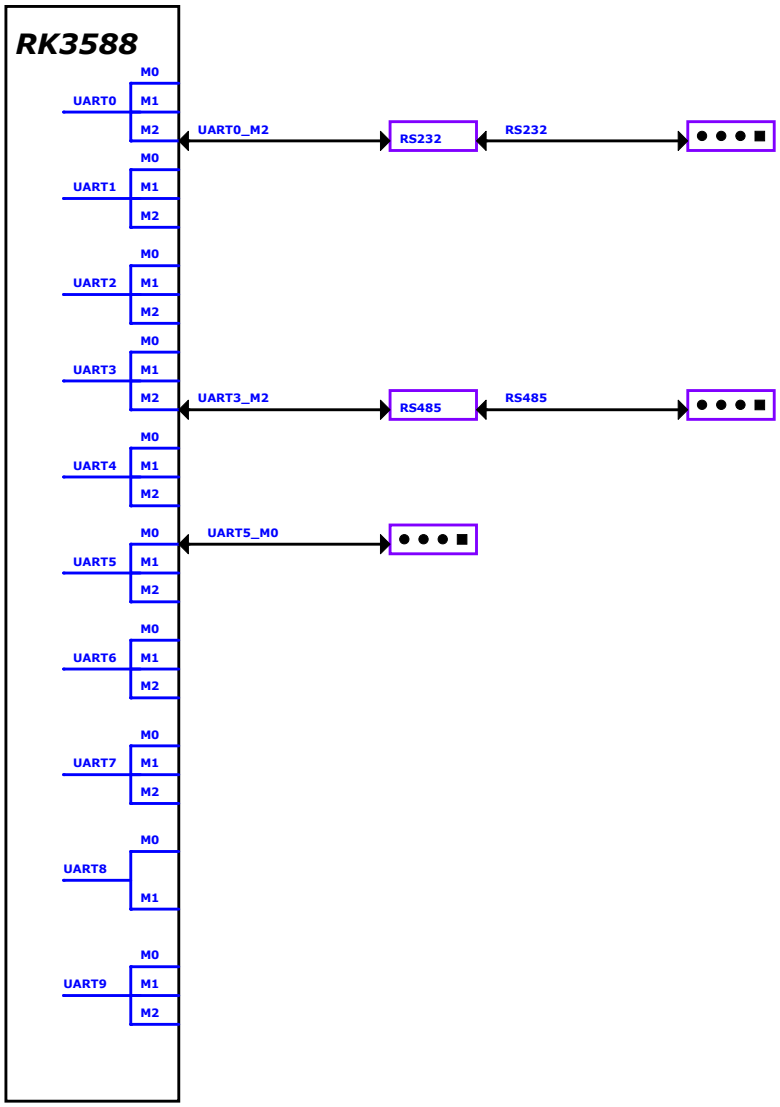
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	05.Power Sequence/IO Domain Map				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	6 of 43

I2C MAP



UART MAP



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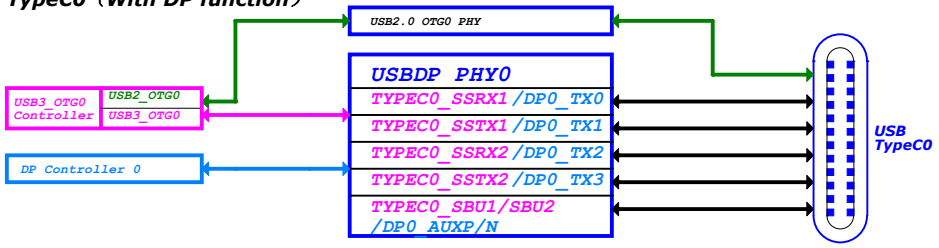
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	05.Lower-Speed Bus Map
Date:	Friday, August 12, 2022
Rev:	V2.1
Designed by:	Zhangdz
Reviewed by:	
Sheet:	7 of 43

USB Controller Configure Table

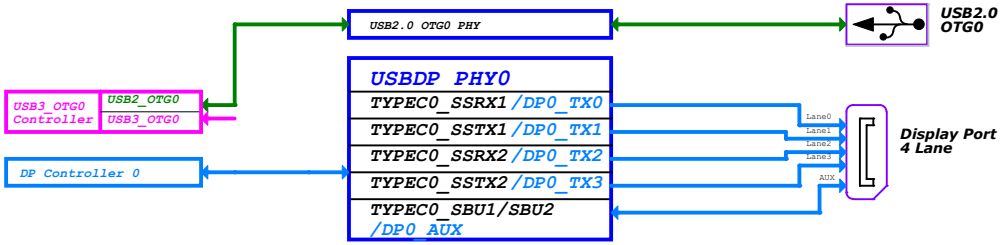
Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST	OPTION3 USB30 HOST				
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN				
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN				
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					
						TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM				

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

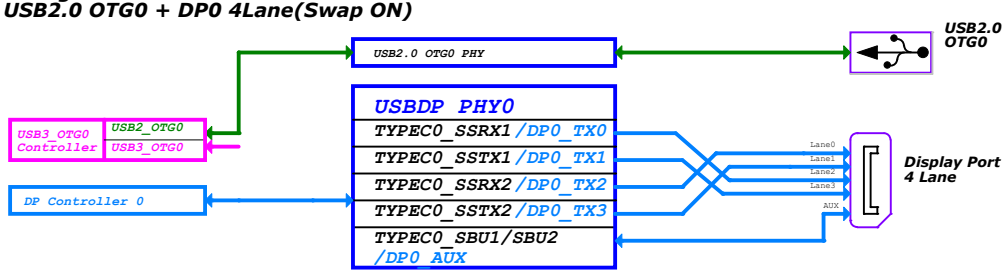
Config0:
TypeC0（With DP function）



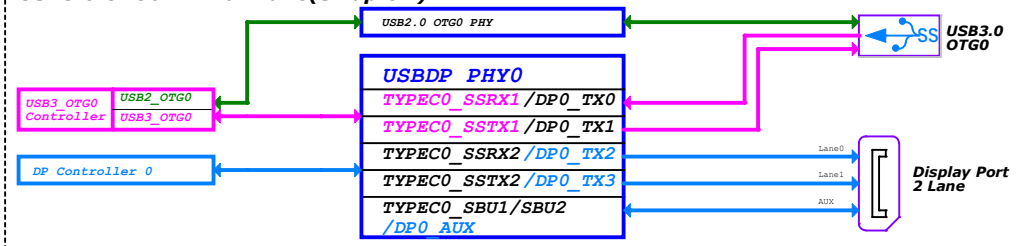
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



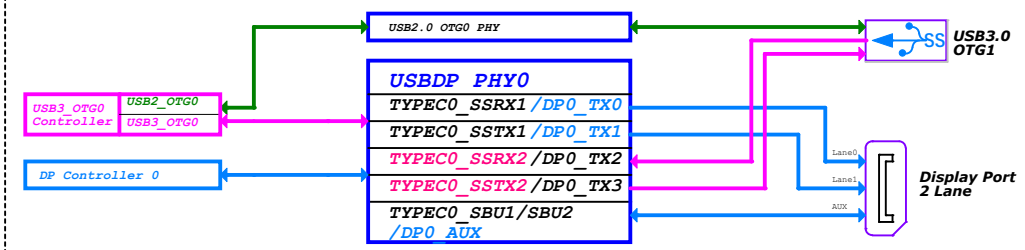
Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Config3:
USB3.0 OTG0 + DP0 2Lane(Swap ON)

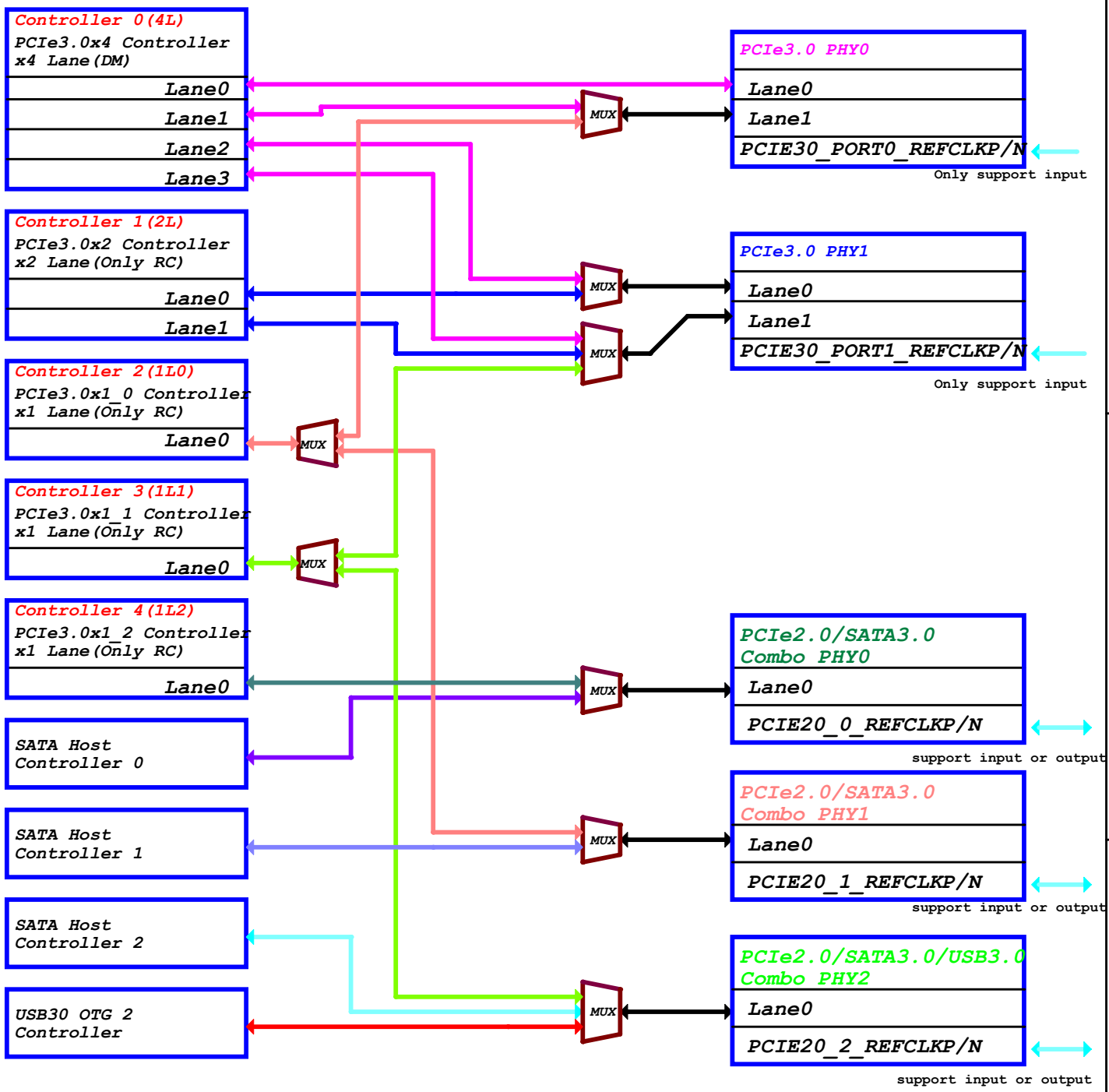


Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	07.USBDP Configure Map
Date:	Friday, August 13, 2021
Designed by:	Reviewed by:
Rev:	V2.1
Sheet:	9 of 43

PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO & Power Pin
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M*
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M*
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

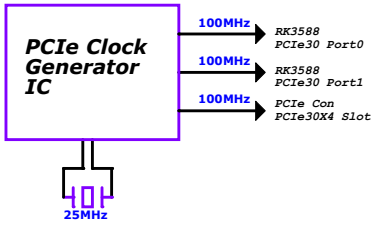
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

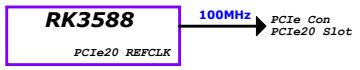
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



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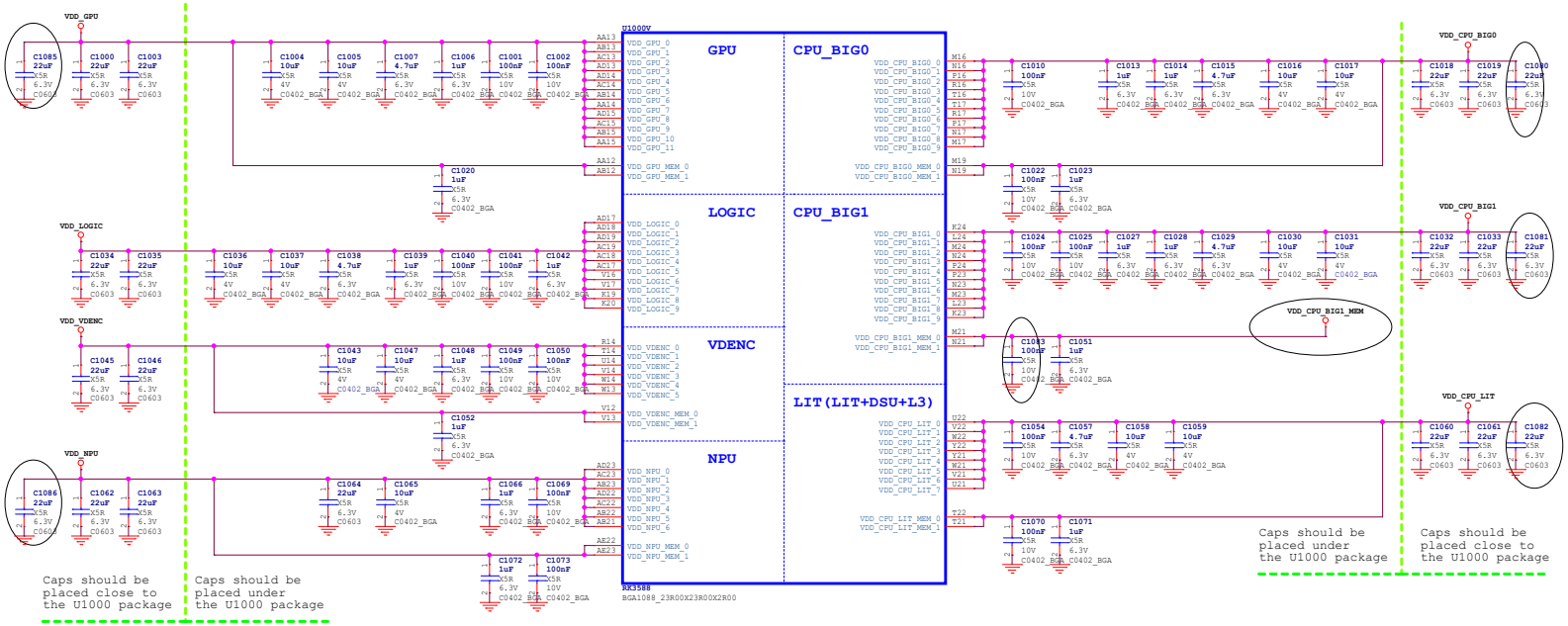
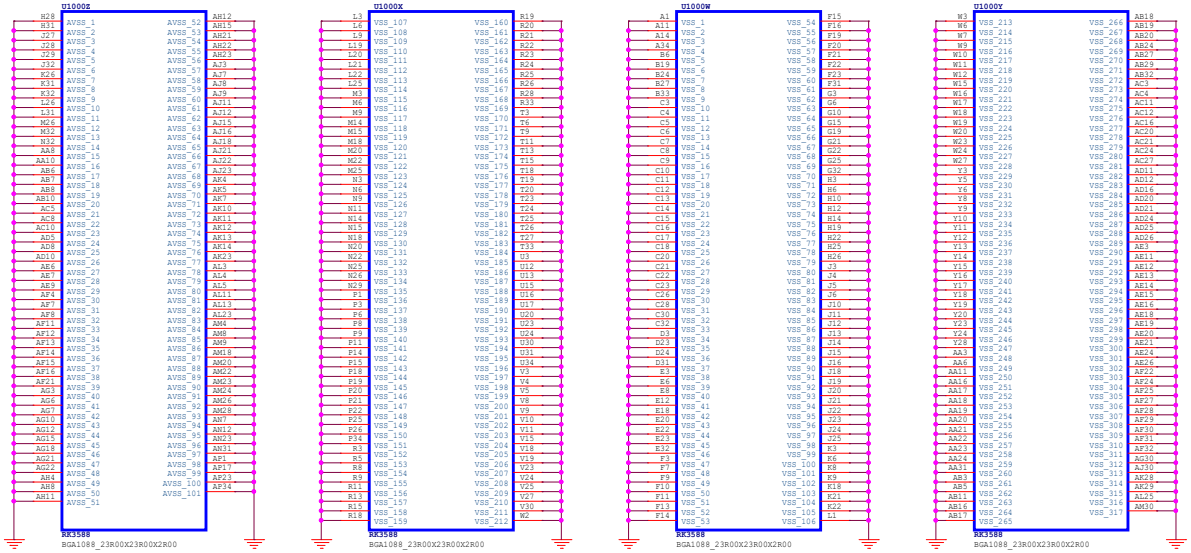
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	08.PCIE Fun Map		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by:	Zhangdt	Reviewed by:	Sheet: 9 of 43





Rockchip Confidential

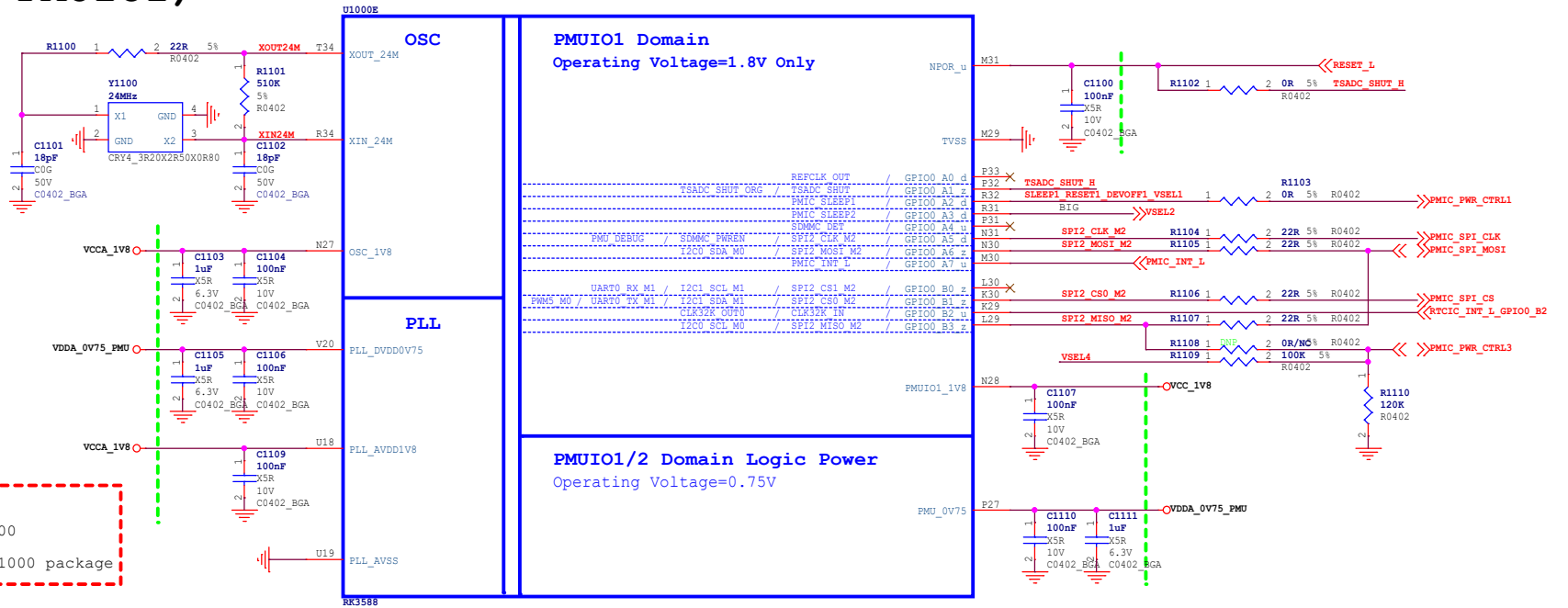
Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	10.RK3588_Power/GND		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by:	Zhangdt	Reviewed by:	Sheet: 10 of 43

RK3588_E(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

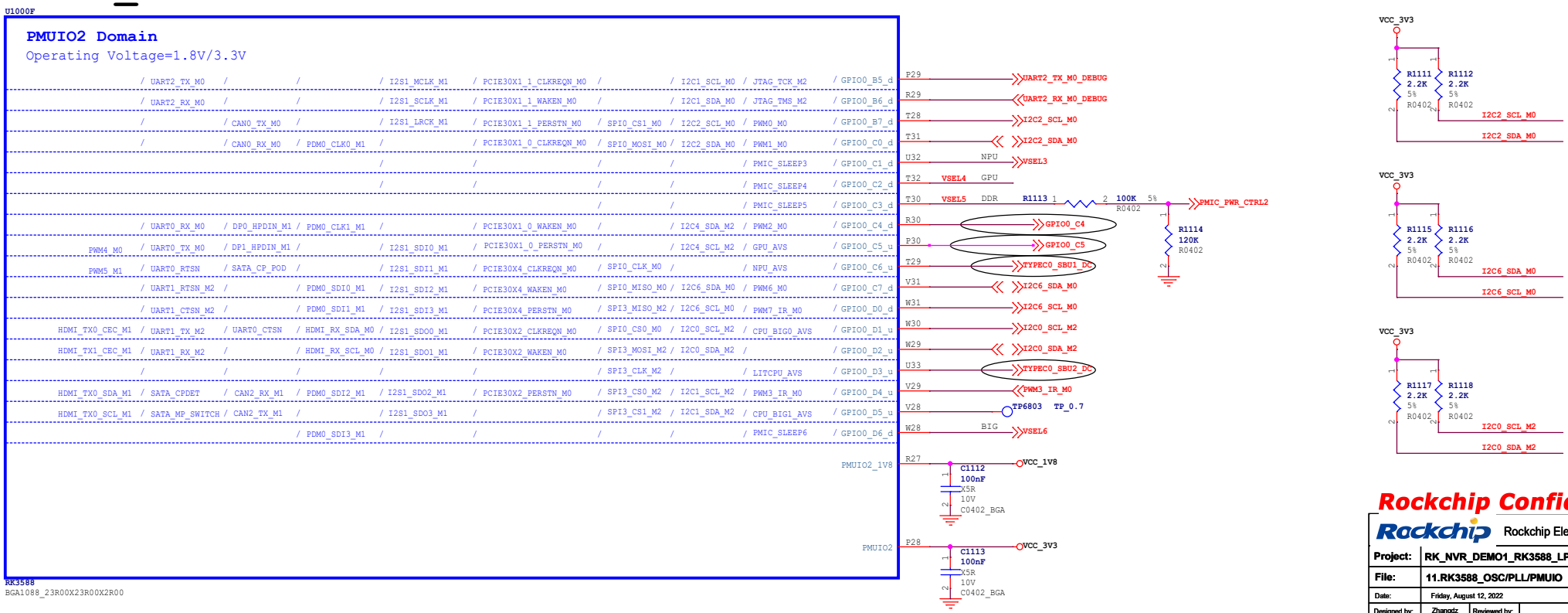
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<12pF

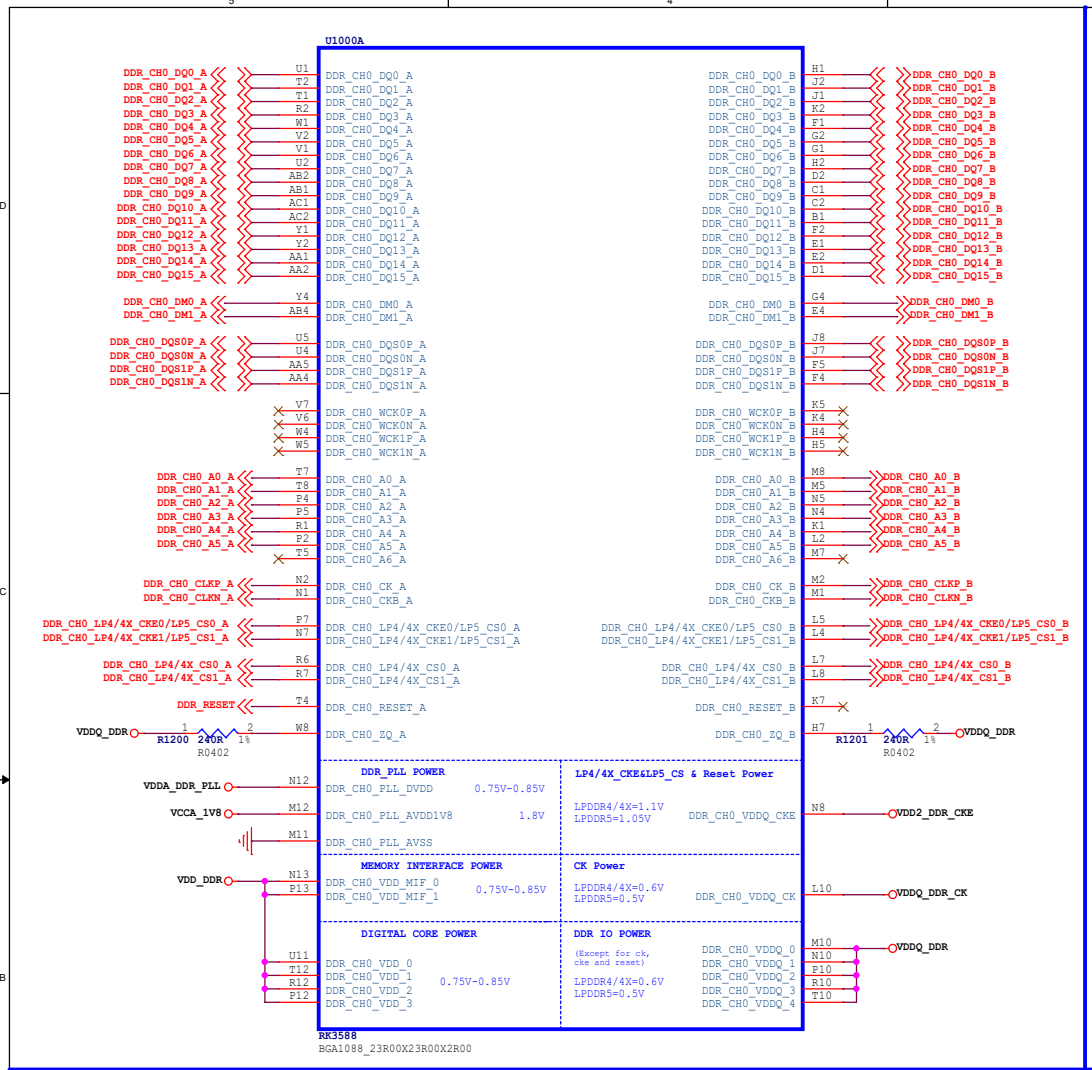


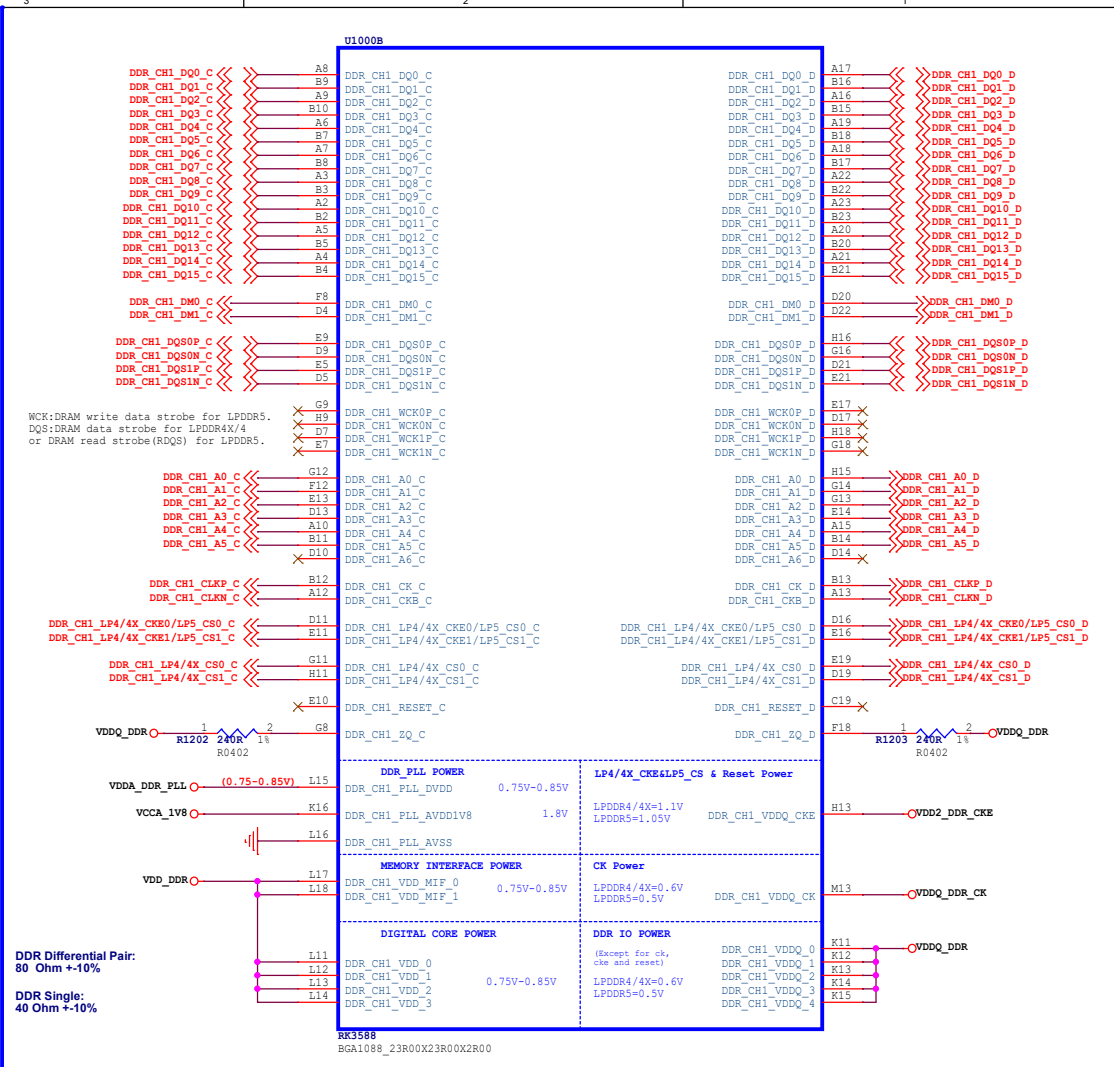
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3588_F(PMUIO2)

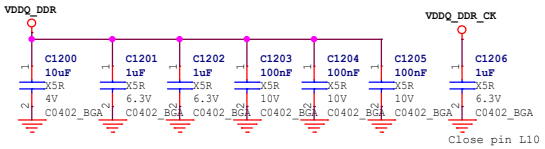


Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	11.RK3588_OSC/PLL/PMUIO		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Sheet: 11 of 43





DDR FILTER



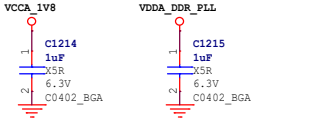
Hold power of CLK during retention times.

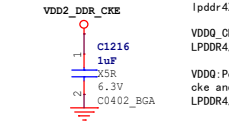
Sequence:
VDD-VDDQ_CKE-VDDQ

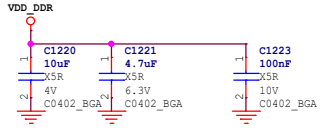
VDDQ_LP4/4X_CKE/LP5_CS:
power for LP4_CKE/LP5_CS and RESET,
lpddr4X=1.1V/lpddr5=1.05V

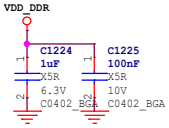
VDDQ_CK:power for CK,
LPDDR4/4X=0.6V/LPDDR5=0.5V

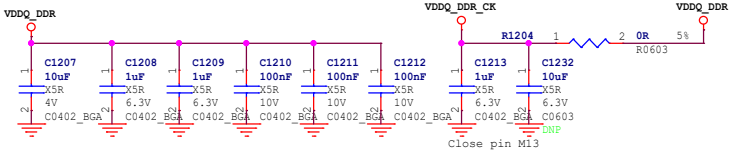
VDDQ:Power for DDR IO(except for ck, cke and reset);
LPDDR4/4X=0.6V/LPDDR5=0.5V

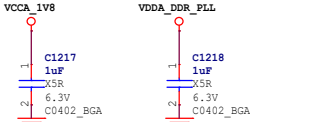


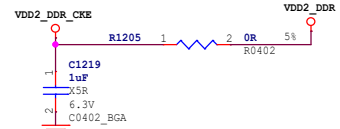


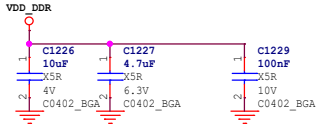


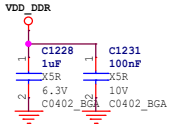












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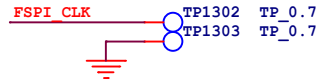
Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	12.RK3588 DDR Controler				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	12 of 43

RK3588_C(EMMCIO Domain)



U1000C

EMMCIO Domain

Operating Voltage=1.8V

	FSPI_D0_M0	/ EMMC_D0	/ GPIO2_D0_u	Y33 eMMC_D0/FSPI_D0
	FSPI_D1_M0	/ EMMC_D1	/ GPIO2_D1_u	W33 eMMC_D1/FSPI_D1
	FSPI_D2_M0	/ EMMC_D2	/ GPIO2_D2_u	V32 eMMC_D2/FSPI_D2
	FSPI_D3_M0	/ EMMC_D3	/ GPIO2_D3_u	AA33 eMMC_D3/FSPI_D3
UART5_RX_M2	/ I2C1_SCL_M3	/ EMMC_D4	/ GPIO2_D4_u	Y32 eMMC_D4_SOC
UART5_TX_M2	/ I2C1_SDA_M3	/ EMMC_D5	/ GPIO2_D5_u	AA32 eMMC_D5_SOC
	FSPI_CS0N_M0	/ EMMC_D6	/ GPIO2_D6_u	W32 eMMC_D6/FSPI_CS0
	FSPI_CS1N_M0	/ EMMC_D7	/ GPIO2_D7_u	V33 eMMC_D7_SOC
	FSPI_CLK_M0	/ EMMC_CMD	/ GPIO2_A0_u	W34 eMMC_CMD/FSPI_CLK
		/ EMMC_CLKOUT	/ GPIO2_A1_d	V34 eMMC_CLKOUT_SOC
UART5_CTSN_M1	/ I2C2_SDA_M2	/ EMMC_DATA_STROBE	/ GPIO2_A2_d	Y34
UART5_RTSN_M1	/ I2C2_SCL_M2	/ EMMC_RSTN	/ GPIO2_A3_d	AA34 eMMC_RSTn_SOC
			EMMCIO_1V8	V26

RK3588

BGA1088_23R00X23R00X2R00

eMMC_D4
eMMC_D5
eMMC_D7

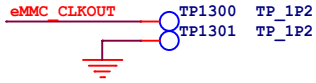
R1310 1 — 2 22R R0402 5%

eMMC_CLKOUT
eMMC_DATA_STROBE
eMMC_RSTn

C1300 1uF X5R 6.3V C0402_BGA

VCC_1V8

eMMC_D0/FSPI_D0 — eMMC_D0
eMMC_D1/FSPI_D1 — eMMC_D1
eMMC_D2/FSPI_D2 — eMMC_D2
eMMC_D3/FSPI_D3 — eMMC_D3
eMMC_CMD/FSPI_CLK — eMMC_CMD
eMMC_D6/FSPI_CS0 — eMMC_D6



RK3588_D(VCCIO2 Domain)

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

U1000D

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

PWM8_M1	/I2C3_SCL_M4	/PDM1_SDI3_M0 / JTAG_TCK_M1	/UART2_TX_M1	/ SDMMC_D0 / GPIO4_D0_u
PWM9_M1	/I2C3_SDA_M4	/PDM1_SDI2_M0 / JTAG_TMS_M1	/UART2_RX_M1	/ SDMMC_D1 / GPIO4_D1_u
	/I2C8_SCL_M0	/PDM1_SDI1_M0 / JTAG_TCK_M0	/UART5_CTSN_M0	/ SDMMC_D2 / GPIO4_D2_u
PWM10_M1	/I2C8_SDA_M0	/PDM1_SDI0_M0 / JTAG_TMS_M0	/UART5_RTSN_M0	/ SDMMC_D3 / GPIO4_D3_u
PWM7_IR_M1	/CAN0_TX_M1	/PDM1_CLK1_M0 / MCU_JTAG_TCK_M0	/UART5_RX_M0	/ SDMMC_CMD / GPIO4_D4_u
TEST_CLKOUT_M0	/CAN0_RX_M1	/PDM1_CLK0_M0 / MCU_JTAG_TMS_M0	/UART5_TX_M0	/ SDMMC_CLK / GPIO4_D5_d
				AD2
				AD1
				AF2
				AF1
				AE2
				AE1
			VCCIO2_1V8	AA7
			VCCIO2	Y7

SDIO_D0_M0_WIFI
SDIO_D1_M0_WIFI
SDIO_D2_M0_WIFI
SDIO_D3_M0_WIFI
SDIO_CMD_M0_WIFI
SDIO_CLK_M0_WIFI

C1301 100nF X5R 10V C0402_BGA

C1302 100nF X5R 10V C0402_BGA

VCC_1V8

RK3588

BGA1088_23R00X23R00X2R00

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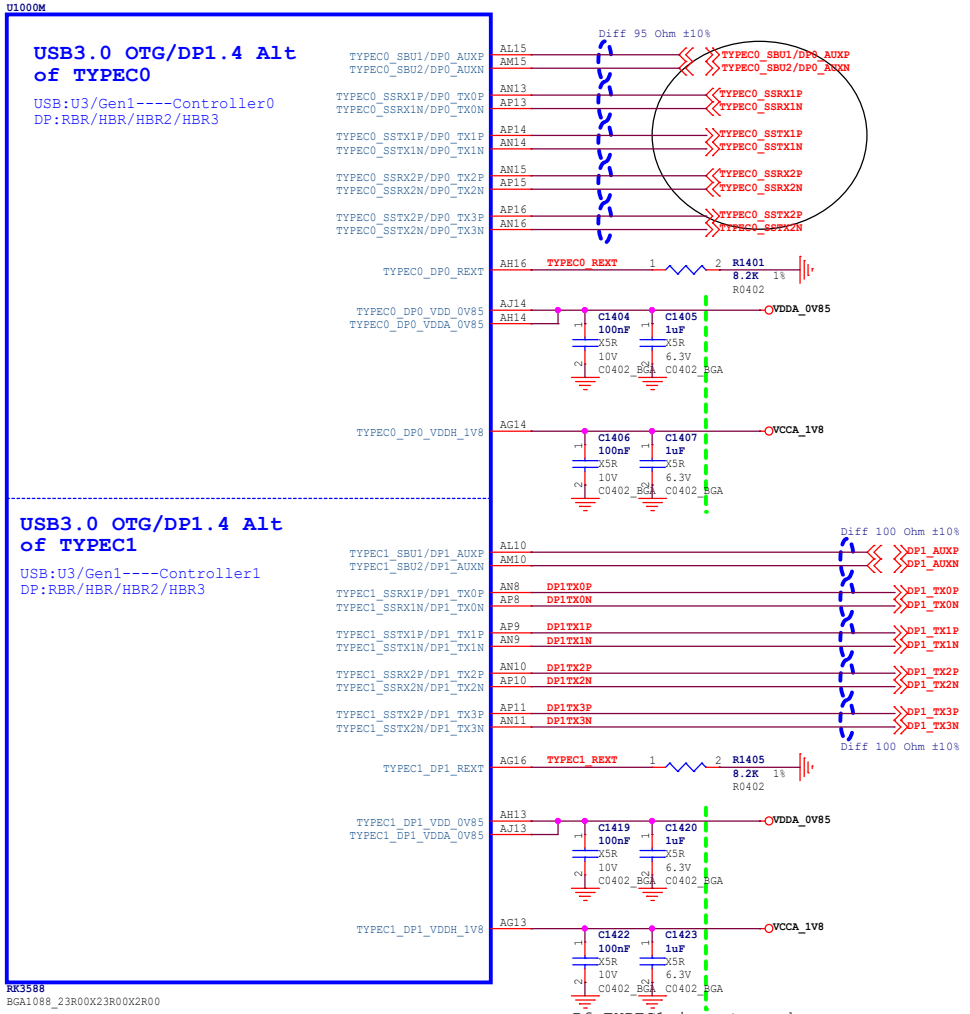
Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	13.RK3588_Flash/SD Controller				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	13 of 43

RK3588_M(TYPEC/DP)

If TYPEC0 is not used,
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power



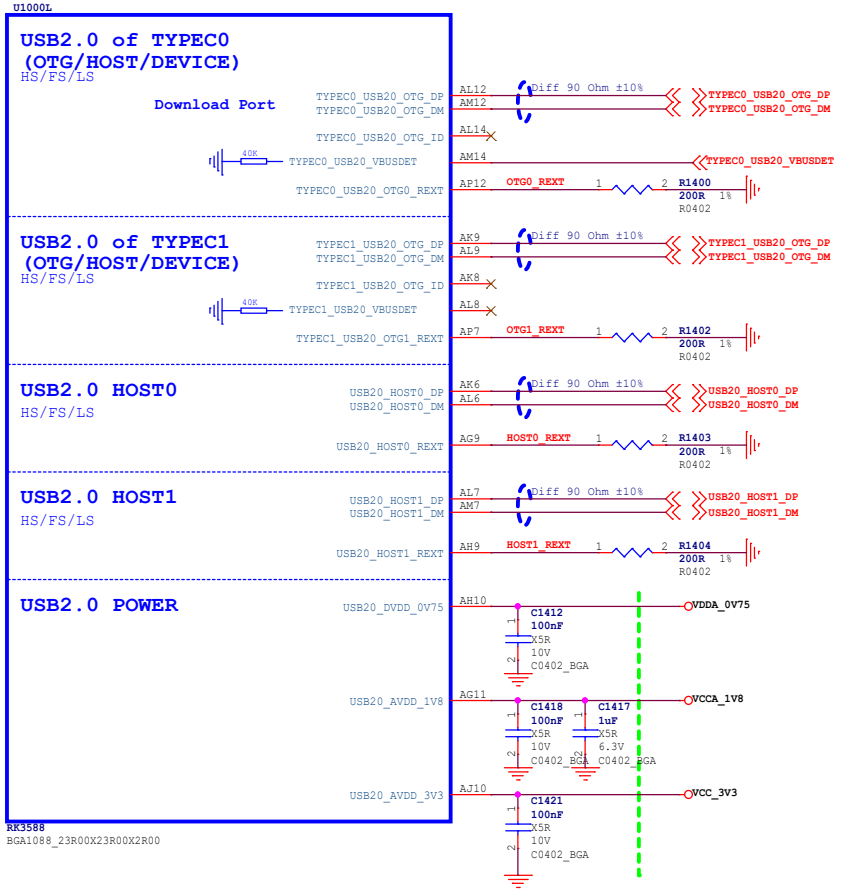
If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588_L(USB2.0 HOST/OTG)



Note:

TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:

If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating

USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:

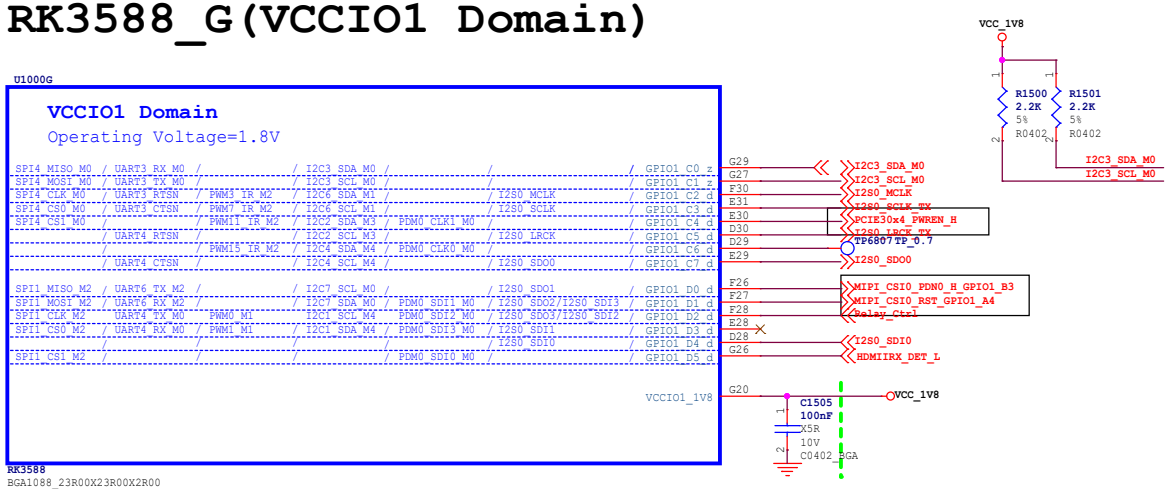
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:

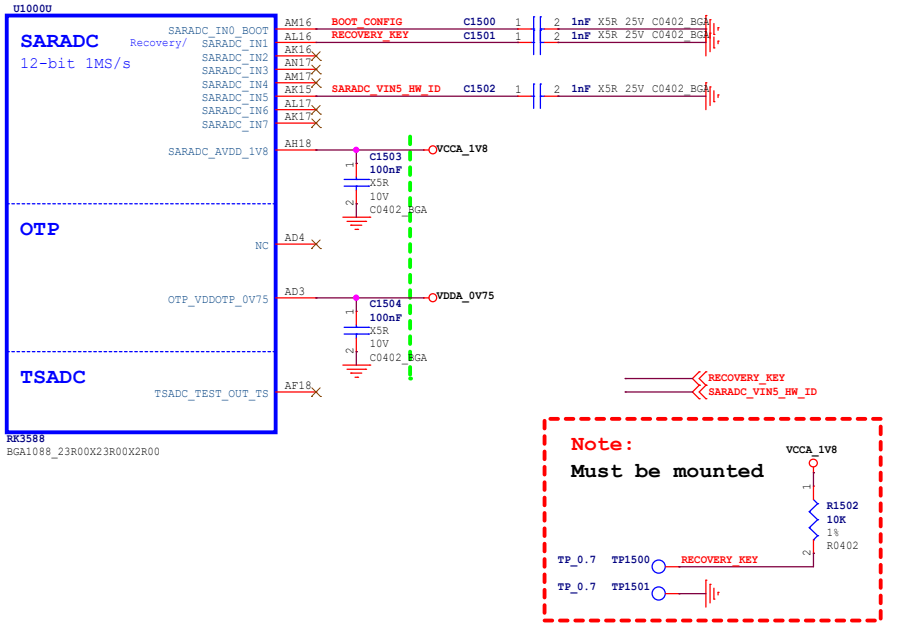
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	14.RK3588_USB30/USB20_Ctrl				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	14 of 43

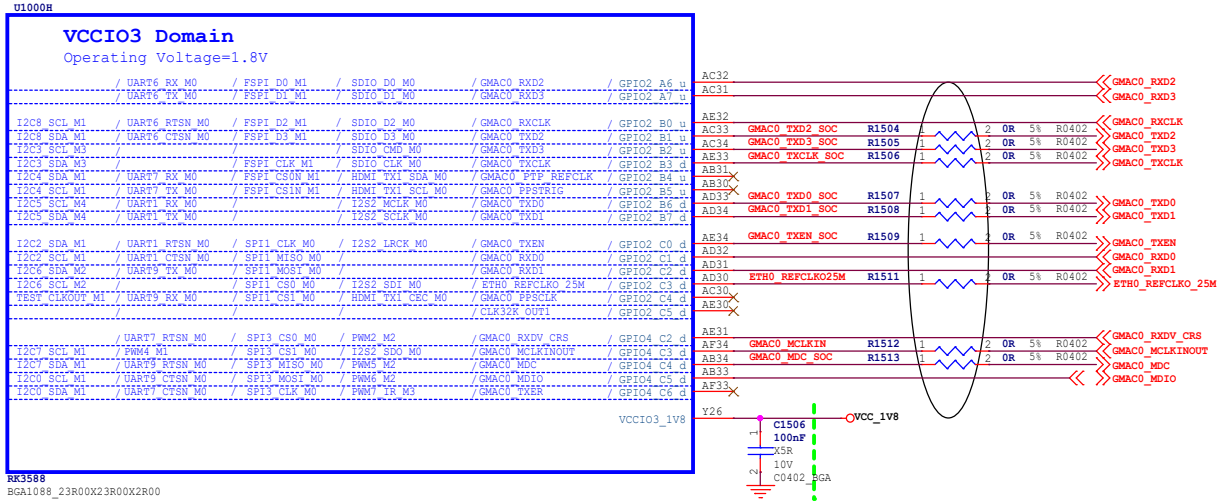
RK3588_G(VCCIO1 Domain)



RK3588_U(SARADC/OTP)

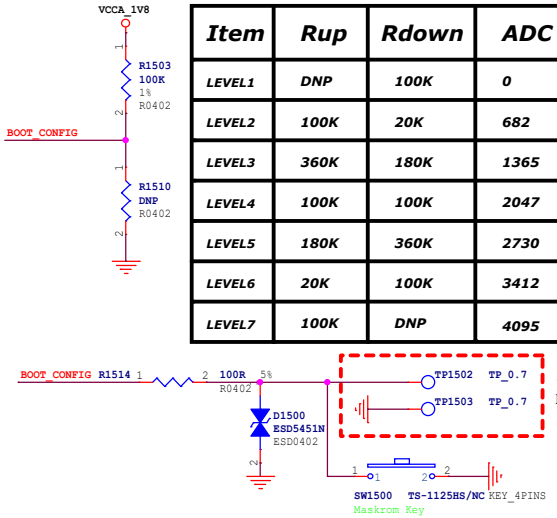


RK3588_H(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

BOOT MODE CONFIG



Item	Rup	Rdown	ADC	VOL	Boot sequence
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

It is recommended to reserve this circuit to enter the MaskROM state for update firmware

Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	15.RK3588_SARADC/1.8V Only GPIO		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by: Zhangdz	Reviewed by:	Sheet:	15 of 43

RK3588_Q/R(MIPI_D/C_PHY0/1)

If not used,
Signal:leave floating
Power: leave floating

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	AN26
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	AP26
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	AN24
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	AP24
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	AN25
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	AP25
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	AN27
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	AP27
MIPI_DPHY0_TX_D3P/NO_USE	AN28
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	AP28

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	AN32
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	AP31
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	AN29
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	AP29
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	AN30
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AP30
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AN33
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	AP32
MIPI_DPHY0_RX_D3P/NO_USE	AN34
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AP33

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG	AF20
MIPI_D/C_PHY0_VDD	AG20
MIPI_D/C_PHY0_VDD_1V2	AH20
MIPI_D/C_PHY0_VDD_1V8	AJ20

RK3588
BGA1088_23R00X23R00X2R00

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	AN20
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	AP20
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	AN18
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	AP18
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	AN19
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	AP19
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	AN21
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	AP21
MIPI_DPHY1_TX_D3P/NO_USE	AN22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	AP22

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	AK20
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	AL20
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	AK18
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	AL18
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	AK19
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	AL19
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	AK21
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	AL21
MIPI_DPHY1_RX_D3P/NO_USE	AK22
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	AL22

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG	AF19
MIPI_D/C_PHY1_VDD	AG19
MIPI_D/C_PHY1_VDD_1V2	AH19
MIPI_D/C_PHY1_VDD_1V8	AJ19

RK3588
BGA1088_23R00X23R00X2R00

RK3588_P(MIPI_CSI_RX_PHY)

If not used,
Signal:leave floating
Power: leave floating or tie to VSS

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P	AJ33
MIPI_CSI0_CLK0N	AJ34
MIPI_CSI0_D0P	AG33
MIPI_CSI0_D0N	AG34
MIPI_CSI0_D1P	AH33
MIPI_CSI0_D1N	AH34
MIPI_CSI0_CLK1P	AM33
MIPI_CSI0_CLK1N	AM34
MIPI_CSI0_D2P	AK33
MIPI_CSI0_D2N	AK34
MIPI_CSI0_D3P	AL33
MIPI_CSI0_D3N	AL34
MIPI_CSI0_AVCC0V75	AB25
MIPI_CSI0_AVCC1V8	AB26

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P	AJ31
MIPI_CSI1_CLK0N	AJ32
MIPI_CSI1_D0P	AG31
MIPI_CSI1_D0N	AG32
MIPI_CSI1_D1P	AH31
MIPI_CSI1_D1N	AH32
MIPI_CSI1_CLK1P	AM31
MIPI_CSI1_CLK1N	AM32
MIPI_CSI1_D2P	AK31
MIPI_CSI1_D2N	AK32
MIPI_CSI1_D3P	AL31
MIPI_CSI1_D3N	AL32
MIPI_CSI1_AVCC0V75	AA25
MIPI_CSI1_AVCC1V8	AA26

RK3588
BGA1088_23R00X23R00X2R00

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Power merging,
capacitance sharing

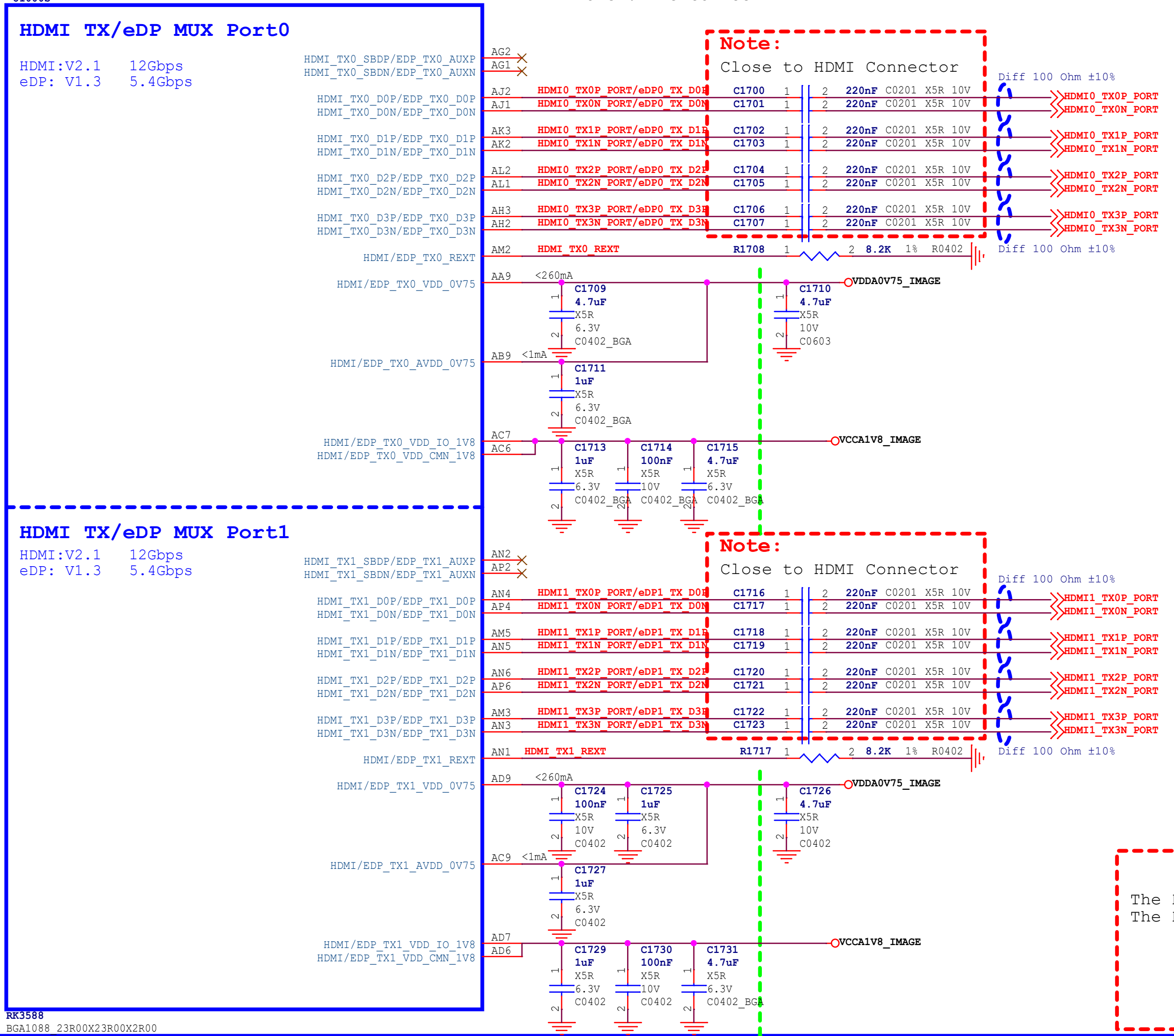
Power merging,
capacitance sharing

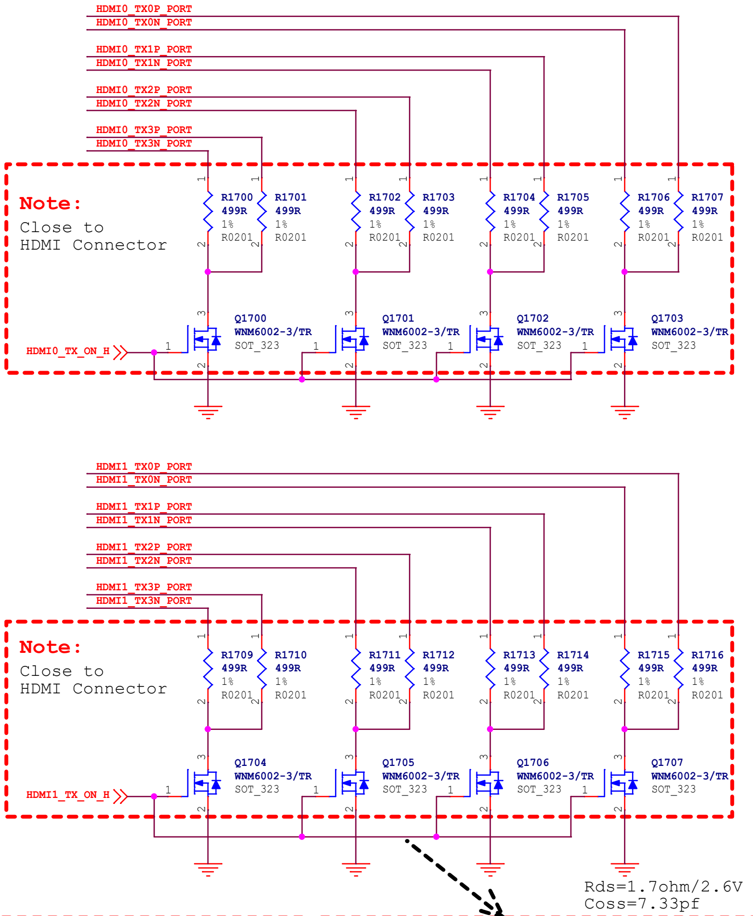
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	16.RK3588_MIPI Interface
Date:	Friday, August 12, 2022
Rev:	V2.1
Designed by:	Zhangdz
Reviewed by:	
Sheet	16 of 43

RK3588_S(HDMI2.1 TX)

If not used,
Signal:leave floating
Power: Tie to VSS





The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

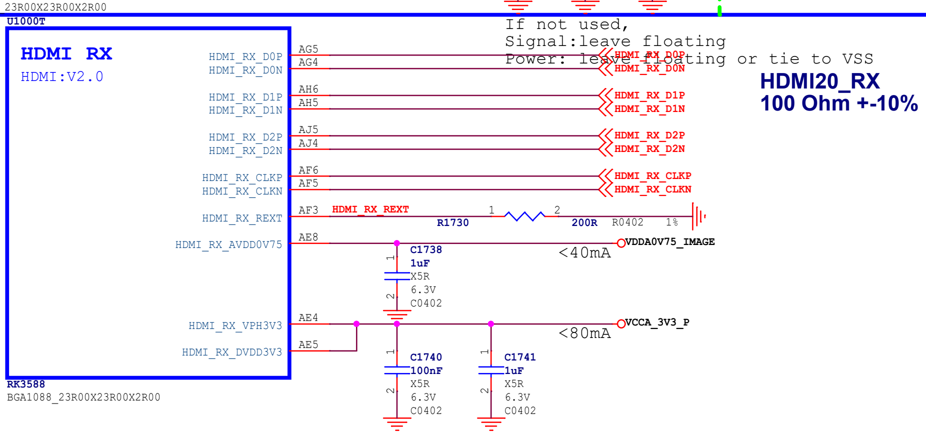
Note:
The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

RK3588_T(HDMI20 RX)

If not used,
Signal:leave floating
Power: leave floating or tie to VSS

HDMI20_RX
100 Ohm +-10%



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd

Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	17.RK3588_HDMI/eDP Interface		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	
Sheet:	17 of 43		

RK3588_N(PCIE20)

If not used,
Signal:leave floating
Power: Tie to VSS

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP
PCIE20_0_REFCLKN
L32
L33
Diff 100 Ohm ±10%

PCIE20_0_TXP/SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN
M34
M33
SATA30_0_TXP
SATA30_0_TXN

PCIE20_0_RXP/SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN
N33
N34
SATA30_0_RXP
SATA30_0_RXN

PCIE20_SATA30_0_AVDD_0V85
M28
VDDA_0V85
C1801
10uF
X5R
4V
C0402_BGA

PCIE20_SATA30_0_AVDD_1V8
M27
VCCA_1V8
C1803
4.7uF
X5R
6.3V
C0402_BGA

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP
PCIE20_1_REFCLKN
H32
H33
PCIE20_1_REFCLKP
PCIE20_1_REFCLKN
Diff 100 Ohm ±10%

PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN
K33
K34
PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN

PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN
J33
J34
PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN

PCIE20_SATA30_1_AVDD_0V85
L28
VDDA_0V85
C1808
100nF
X5R
10V
C0402_BGA

PCIE20_SATA30_1_AVDD_1V8
L27
VCCA_1V8
C1810
100nF
X5R
10V
C0402_BGA

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
G31
G30
Diff 90 Ohm ±10%

PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN
H30
H29
USB30_2_SSTXP
USB30_2_SSTXN

PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN
J31
J30
USB30_2_SSRXP
USB30_2_SSRXN

PCIE20_SATA30_USB30_2_AVDD_0V85
K28
VDDA_0V85
C1816
1uF
X5R
6.3V
C0402_BGA

PCIE20_SATA30_USB30_2_AVDD_1V8
K27
VCCA_1V8
C1819
4.7uF
X5R
6.3V
C0402_BGA

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

Power merging,
capacitance sharing

Power merging,
capacitance sharing

RK3588
BGA1088_23R00X23R00X2R00

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3588_O(PCIE30)

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIE20/SATA30
MUX1

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30
MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input

PCIE30_PORT0_REF_CLKP
PCIE30_PORT0_REF_CLKN
E33
E34

Lane0

PCIE30_PORT0_TX0P
PCIE30_PORT0_TX0N
D32
D33

PCIE30_PORT0_RX0P
PCIE30_PORT0_RX0N
G33
G34

Lane1

PCIE30_PORT0_TX1P
PCIE30_PORT0_TX1N
C33
C34

PCIE30_PORT0_RX1P
PCIE30_PORT0_RX1N
F32
F33

PCIE30_PORT0_RESREF
B34

PCIE30_PORT0_AVDD0V75
G24

PCIE30_PORT0_AVDD1V8
G23

PCIE30 PORT1

input

PCIE30_PORT1_REF_CLKP
PCIE30_PORT1_REF_CLKN
A28
B28

Lane0

PCIE30_PORT1_TX0P
PCIE30_PORT1_TX0N
B30
A30

PCIE30_PORT1_RX0P
PCIE30_PORT1_RX0N
B32
A32

Lane1

PCIE30_PORT1_TX1P
PCIE30_PORT1_TX1N
C29
B29

PCIE30_PORT1_RX1P
PCIE30_PORT1_RX1N
C31
B31

PCIE30_PORT1_RESREF
A33

PCIE30_PORT1_AVDD0V75
H24

PCIE30_PORT1_AVDD1V8
H23

RK3588
BGA1088_23R00X23R00X2R00

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	18 of 43

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1	/	I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1	/	FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1	/	FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1	/	/	I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2	/	SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d
	MIPI_CAMERA1_CLK_M1	/	I2C4_SCL_M0	/	/	/	ETH1_REFCLKO_25M	GPIO3_A6_d
PWM8_M0	MIPI_CAMERA2_CLK_M1	/	/	/	/	/	GMAC1_RXD0	GPIO3_A7_u
PWM9_M0	MIPI_CAMERA3_CLK_M1	/	/	/	/	/	GMAC1_RXD1	GPIO3_B0_u
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2	/	/	/	/	GMAC1_RXDV_CRS	GPIO3_B1_d
PWM3_IR_M1	/	UART2_RX_M2	/	/	I2S2_SDI_M1	/	GMAC1_TXER	GPIO3_B2_d
	/	UART2_RTSN	/	/	I2S2_SDO_M1	/	GMAC1_TXD0	GPIO3_B3_u
	/	UART2_CTSN	/	/	I2S2_MCLK_M1	/	GMAC1_TXD1	GPIO3_B4_u
PWM12_M0	CAN1_RX_M0	UART3_TX_M1	/	/	I2S2_SCLK_M1	/	GMAC1_TXEN	GPIO3_B5_u
PWM13_M0	CAN1_TX_M0	UART3_RX_M1	/	/	I2S2_LRCK_M1	/	GMAC1_MCLKINOUT	GPIO3_B6_d
	/	/	I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1	/	GMAC1_PTP_REF_CLK	GPIO3_B7_d
	/	UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1	/	/	GMAC1_PPSTRIG	GPIO3_C0_d
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1	/	SPI1_CLK_M1	/	/	GMAC1_PPSCLK	GPIO3_C1_d
PWM14_M0	/	UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1	/	MIPI_TE0	GMAC1_MDC	GPIO3_C2_d
PWM15_IR_M0	/	UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1	/	MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2	/	CIF_D8	GPIO3_C4_u
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1	/	CIF_D9	GPIO3_C5_u
	PCIE30X4_PERSTN_M2	/	/	SPI3_MISO_M3	HDMI_TX1_SCL_M1	/	CIF_D10	GPIO3_C6_u
	PCIE20X1_2_CLKREQN_M0	/	I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2	/	CIF_D11	GPIO3_C7_u
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2	/	CIF_D12	GPIO3_D0_u
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1	/	SPI0_MISO_M3	HDMI_RX_CEC_M1	/	CIF_D13	GPIO3_D1_d
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1	/	CIF_D14	GPIO3_D2_d
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1	/	CIF_D15	GPIO3_D3_d
	PCIE30X2_PERSTN_M2	UART9_RX_M2	/	SPI0_CS0_M3	HDMI_RX_HPDOUT_M1/ HDMI_TX0_HPD_M1/	MCU_JTAG_TCK_M1		GPIO3_D4_d
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2	/	SPI0_CS1_M3	DP1_HPDIN_M0	/	MCU_JTAG_TMS_M1	GPIO3_D5_d

AA29	GMAC1_TXD2_SOC	R1900 1	2 0R 5% R0402 GMAC1_TXD2
AA30	GMAC1_TXD3_SOC	R1901 1	2 0R 5% R0402 GMAC1_TXD3
AD27	GMAC1_RXD2_SOC		GMAC1_RXD2
AE27	GMAC1_RXD3_SOC		GMAC1_RXD3
AD28	GMAC1_TXCLK_SOC	R1904 1	0R 5% R0402 GMAC1_TXCLK
AH30	GMAC1_RXCLK_SOC		GMAC1_RXCLK
AH27	ETH1_REFCLKO_25M	R1906 1	0R 5% R0402 ETH1_REFCLKO_25M
AG29			GMAC1_RXD0
AG28			GMAC1_RXD1
AH29			GMAC1_RXDV_CRS
AE28			GPIO3_B2 WZH_0310
AC28	GMAC1_TXD0_SOC	R1907 1	2 0R 5% R0402 GMAC1_TXD0
AC29	GMAC1_TXD1_SOC	R1908 1	2 0R 5% R0402 GMAC1_TXD1
AD29	GMAC1_TXEN_SOC	R1909 1	2 0R 5% R0402 GMAC1_TXEN
AE29	GMAC1_MCLKIN	R1910 1	2 0R 5% R0402 GMAC1_MCLKINOUT
AA28			Power_LED_EN_H_GPIO3_B7
Y29			Ethernet_LED_EN_H_GPIO3_C0
Y27			HDD_LED_EN_H_GPIO3_C1
Y31	GMAC1_MDC_SOC	R1911 1	0R 5% R0402 GMAC1_MDC
Y30			GMAC1_MDIO
AH26	HDMITX1_CEC_M2SOC	R1912 1	2 0R 5% R0402 HDMITX1_CEC_M2
AH25			HDMITX1_SDA_M2
AG26			HDMITX1_SCL_M1 WZH_0310
AJ24			HSSCC_INT_L
AH24			GPIO3_D0
AG23			HDMI_RX_CEC
AG25			HDMI_RX_SCL_M1
AG24			HDMI_RX_SDA_M1
AA27			HDMIIRX_HPDOUT_H
AB28			DP1_HPDIN_M0

VCCIO5_1V8 W25 VCC_1V8

And PinY26 Power merging, capacitance sharing

VCCIO5 W26 VCC_3V3

C1901 100nF X5R 10V C0402_BGA

RK3588 BGA1088_23R00X23R00X2R00

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1	/	I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1	/	I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1	/	/	I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
	/	UART0_TX_M2	/	/	PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2	/	PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2	I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2	I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1	/	I2C5_SDA_M2	I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3	I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3	I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN	/	MIPI_CAMERA0_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3	I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1	/	UART8_CTSN_M0	I2C7_SDA_M3	I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIF0_TX_M1	PWM1_IR_M1	DP0_HPDIN_M0	UART9_TX_M1	/	I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1	/	HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11	/	GPIO4_B5_u
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1	/	I2C5_SCL_M1	HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12	/	GPIO4_B6_d
	/	SPI3_CLK_M1	/	I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13	/	GPIO4_B7_u
	/	SPI3_CS0_M1	/	I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14	/	GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1	/	I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15	/	GPIO4_C1_d

AK30			GPIO4_A0
AL30			GPIO4_A1
AM29			GMAC1_RSTn_L_GPIO4_A2
AL29			UART0_TX_M2
AL28			UART0_RX_M2
AK27			UART3_TX_M2
AL27			UART3_RX_M2
AM27			USB_OTG_PWREN_H_GPIO4_A7
AK26			USB_HOST_PWREN_H_GPIO4_B0
AL24			HDMI0_TX_ON_H
AK25			HDMI1_TX_ON_H
AM25			GMAC0_RSTn_L_GPIO4_B3
AL26			PCIE30X4_CLKREQn_M1_L
AJ26			PCIE30X4_WAKEn_M1_L
AJ27			PCIE30X4_PERSTn_M1_L
AJ28			HDMITX0_SCL_M0
AJ25			HDMITX0_SDA_M0
AK24			HDMITX0_CEC_M0

VCCIO6_1V8 AC25 VCC_1V8

C1902 100nF X5R 10V C0402_BGA

VCCIO6 AC26 VCC_3V3

C1905 100nF X5R 10V C0402_BGA

RK3588 BGA1088_23R00X23R00X2R00

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2	I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d
SATA1_ACT_LED_M1	/	SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2	I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d
	PWM0_M2	SPI4_CLK_M2	/	VOP_POST_EMPTY	I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d
	PWM1_M2	SPI4_CS0_M2	/	HDMI_TX1_SDA_M2	I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d
	/	SPI2_MISO_M0	/	HDMI_TX1_SCL_M2	/	/	GPIO1_A4_d
	/	SPI2_MOSI_M0	/	HDMI_TX0_HPD_M0	/	/	GPIO1_A5_d
	/	SPI2_CLK_M0	/	HDMI_TX1_HPD_M0	/	/	GPIO1_A6_d
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2	/	PDM1_SDI0_M1	/	GPIO1_A7_u
	/	SPI2_CS1_M0	PCIE30X4_CLKREQN_M3	/	PDM1_SDI1_M1	/	GPIO1_B0_u
	/	SPI0_MISO_M2	PCIE30X4_WAKEN_M3	/	PDM1_SDI2_M1	/	GPIO1_B1_d
	/	SPI0_MOSI_M2	PCIE30X4_PERSTN_M3	/	PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d
SATA0_ACT_LED_M1	/	SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2	/	PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d
	/	SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2	/	PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u
	/	SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2	/	/	UART7_TX_M2	GPIO1_B5_u
	HDMI_RX_HPDOUT_M2	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0	I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u
	HDMI_RX_SCL_M2	PWM14_M2	/	/	MIPI_CAMERA3_CLK_M0	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u
	HDMI_RX_SDA_M2	PWM15_IR_M3	/	PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u

A24			UART6_RX_M1_BT
A25			UART6_TX_M1_BT
A26			UART6_RTSn_M1_BT
A27			UART6_CTSn_M1_BT
B25			HOST_WAKE_BT_H
B26			HDMITX0_HPDIN_M0
C24			HDMITX1_HPDIN_M0
C25			WIFI_WAKE_HOST_H
C27			BT_WAKE_HOST_H
D25			WIFI_REG_ON_H
D26			BT_REG_ON_H
D27			PCIEx1_0_WAKEn_M1_L
E24			PCIEx1_0_PERSTn_M1_L
E25			PCIEx1_0_CLKREQn_M1_L
E26			I2C5_SCL_M3_MIPI
E27			I2C5_SDA_M3_MIPI
F24	R1917 1	2 22R 5% R0402	MIPI_CAM3_CLKOUT
F25	R1918 1	2 22R 5% R0402	MIPI_CAM4_CLKOUT

VCCIO4_1V8 H20 VCC_1V8

C1903 100nF X5R 10V C0402_BGA

VCCIO4 H21

RK3588 BGA1088_23R00X23R00X2R00

VCC_1V8

R1913 10K 5% R0402 UART6_RX_M1_BT

R1914 10K 5% R0402 UART6_TX_M1_BT

R9914 10K 5% R0402 UART6_RTSn_M1_BT

R9915 10K 5% R0402 UART6_CTSn_M1_BT

R1915 2.2K 5% R0402 I2C5_SCL_M3_MIPI

R1916 2.2K 5% R0402 I2C5_SDA_M3_MIPI

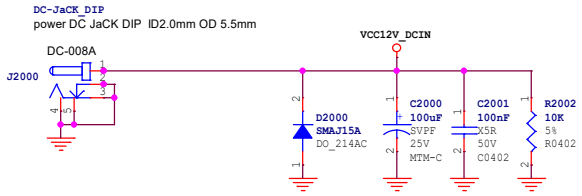
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

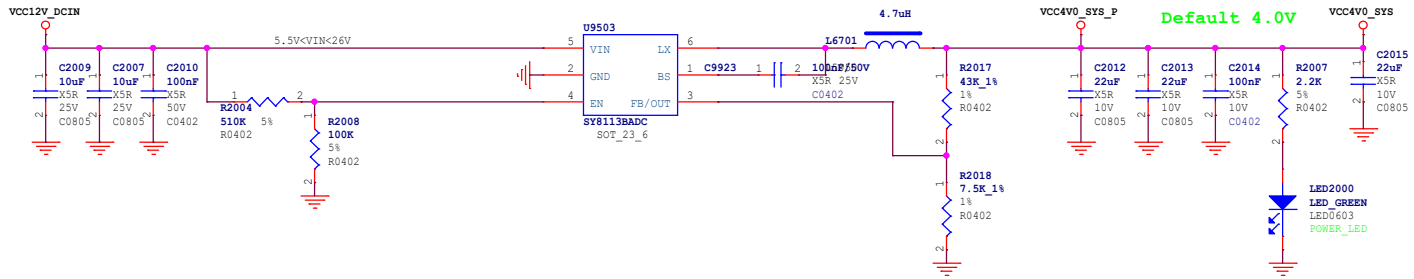
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	19.RK3588_1.8V/ 3.3V GPIO		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by:	Zhangdt	Reviewed by:	Sheet: 19 of 43

12V/3A DCIN

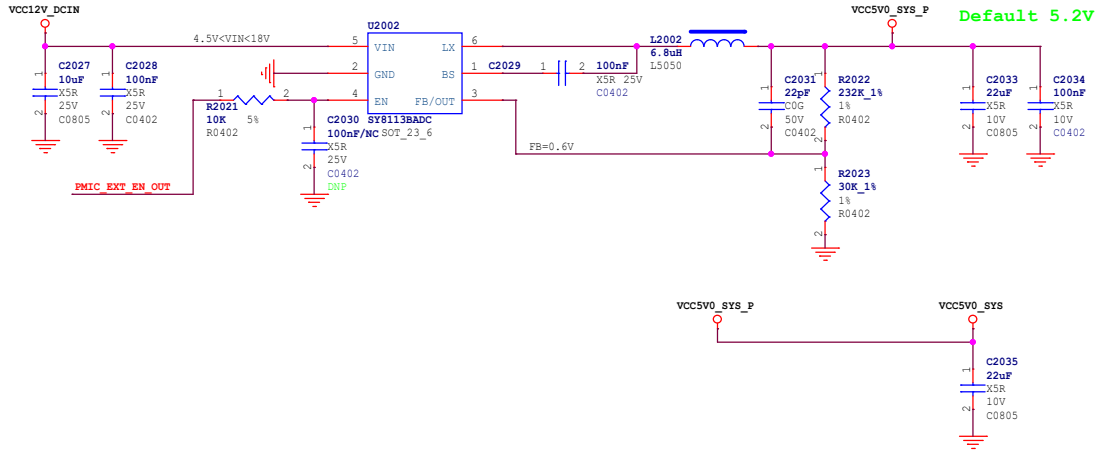
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe



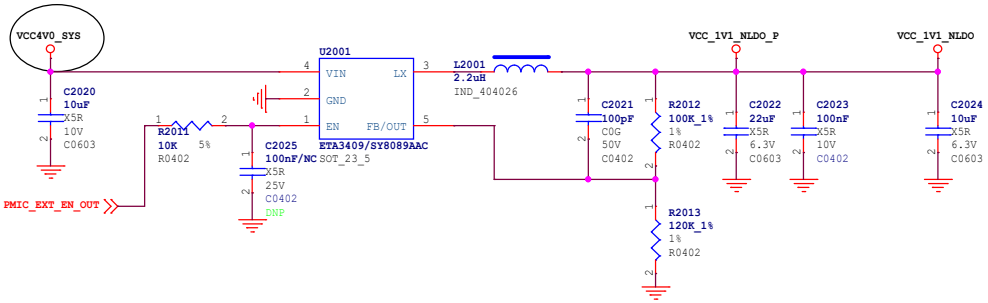
VCC4V0_SYS



VCC5V0_SYS



VCC_1V1_NLDO



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	20.Power_DC IN				
Date:	Tuesday, January 09, 2024			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 43

PMIC RK806-1 BUCK

PMIC_SPI_CS
PMIC_SPI_MOSI
PMIC_SPI_CLK
PMIC_PWR_CTRL1
PMIC_PWR_CTRL2
PMIC_PWR_CTRL3
PMIC_INT_L
RESET_L
PMIC_EXT_EN_OUT

U2200A

BUCK5 2.5A / BUCK1 6.5A
BUCK6 2.5A / BUCK2 5A
BUCK9 2.5A / BUCK3 5A
BUCK8 2.5A / BUCK4 5A
BUCK10 2.5A / BUCK7 2.5A

RK806-1
QFN68_7R00X7R00X0R80_T

Default:0.85V
Low frequency:
0.85V-->0.75V
VDD_DDR
Feedback from RK3588

Default:1.1V
VDD2_DDR
VDD2_DDR_P

LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

Default 0 ohm.
If need end feedback,
need change to 100ohm
Reserved for end feedback

Default:0.6V
VDDQ_DDR
VDDQ_DDR_P
VDDQ_DDR
Feedback from RK3588

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

Default:3.3V
VCC_3V3
VCC_3V3_P

Default:1.8V
VCC_1V8
VCC_1V8_P

VCC4V0_SYS
VDD_GPU
VDD_GPU_P
VDD_CPU_LIT
VDD_CPU_LIT_P
VDD_LOGIC
VDD_LOGIC_P
VDD_VDENC
VDD_VDENC_P
VCC_2V0_PLDO
VCC_2V0_PLDO_P
Default:2.0V

DCDC
OUT
FB
VDD
RK3588

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

ED2200
AZ5825-01F
ESD0402

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage : 5.5V(5.25~6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

PMIC RK806-1 Managerment

U2200C

VCCIO
VCCA

Default:1.8V
VCCA1V8_PLDO6
VCC4V0_SYS
C5925 4.7uF V1.1 220812@wzh
R2212 100K
R2215 100K
C2262 1nF
PWRON_L
V1.1 220812@wzh

PMIC_SPI_CS
PMIC_SPI_MOSI
PMIC_SPI_CLK
PMIC_PWR_CTRL3
PMIC_PWR_CTRL2
PMIC_PWR_CTRL1
PMIC_EXT_EN_OUT
PMIC_INT_L
RESET_L

R2211 100K
R2210 100K/NC
R2213 10K
R2214 10K
C2263 10nF

RK806-1
QFN68_7R00X7R00X0R80_T

RK3588
nPOR
TSADC_SHUT

RK806-1
RESETB

Reset Key

Note:

- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

PLDO
NLDO

VCC_2V0_PLDO
VCC4V0_SYS
VCC_1V1_NLDO
VCC_1V1_NLDO

PLDO1	0.5A
PLDO2	0.3A
PLDO3	0.3A
PLDO4	0.5A
PLDO5	0.3A
NLDO1	0.3A
NLDO2	0.3A
NLDO3	0.5A
NLDO4	0.5A
NLDO5	0.3A

VCCA_1V8
Default:1.8V
VCCA1V8_IMAGE_P
VCCA1V8_IMAGE
Default:1.8V
VCCA1V2_IMAGE
Default:1.2V
VCCA_3V3_P
VCCA_3V3
Default:3.3V
VCCIO_SD_P
Default:3.3V
VDDA_0V75_PMU_P
VDDA_0V75_PMU
Default:0.75V
VDDA_DDR_PLL_P
VDDA_DDR_PLL
Default:0.85V;Low frequency:0.85V-->0.75V
VDDA0V75_IMAGE_P
VDDA0V75_IMAGE
Default:0.75V
VDDA_0V85_P
VDDA_0V85
Default:0.85V
VDDA_0V75_P
VDDA_0V75
Default:0.75V

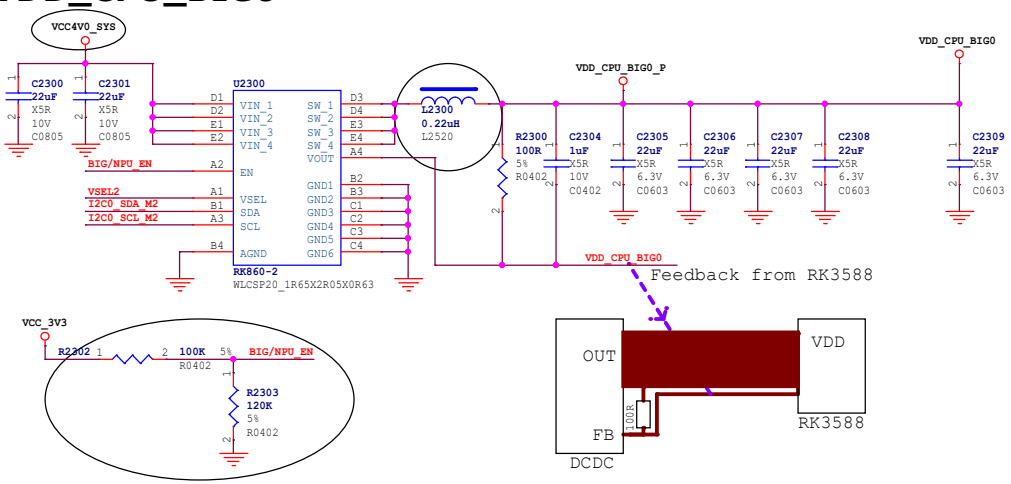
RK806-1
QFN68_7R00X7R00X0R80_T

Note:

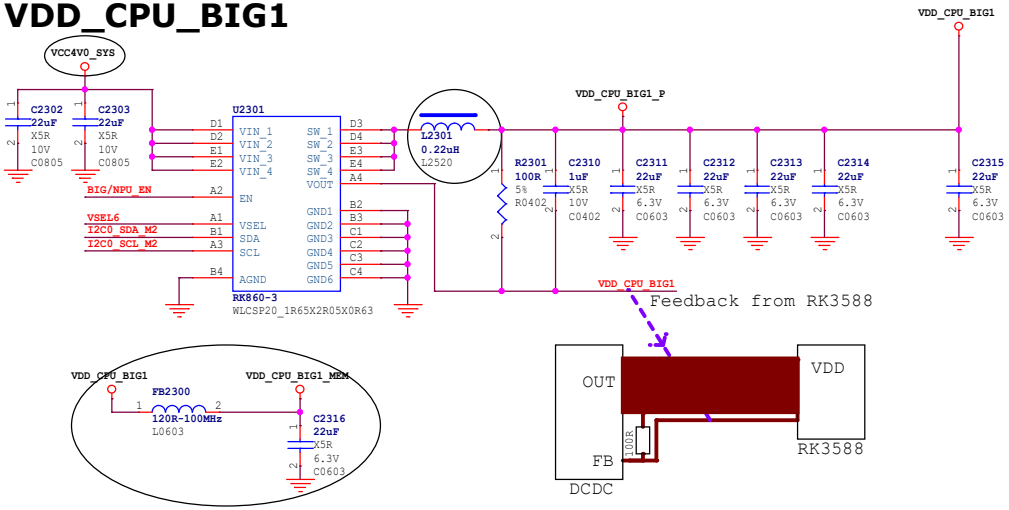
The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	22.Power-PMIC_RK806-1
Date:	Friday, August 12, 2022
Rev:	V2.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	21 of 43

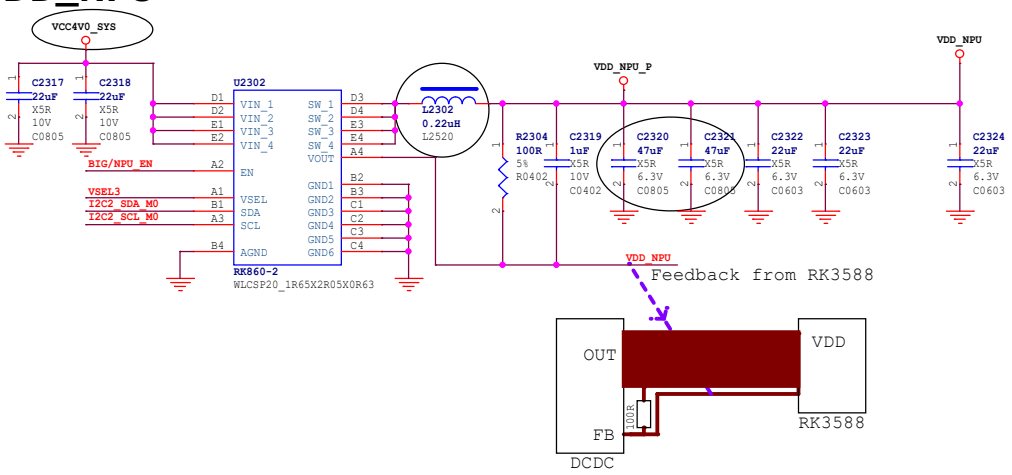
VDD_CPU_BIG0



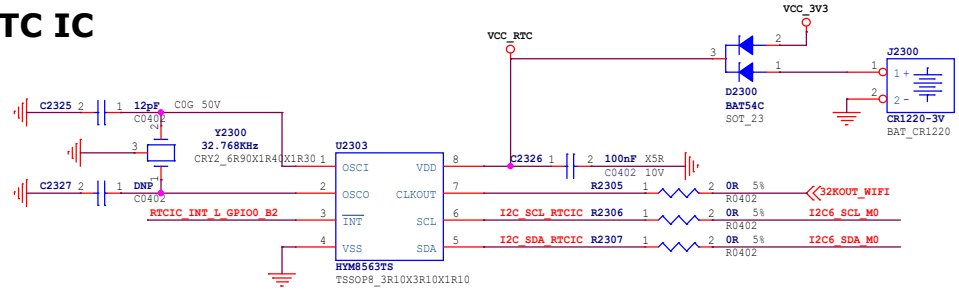
VDD_CPU_BIG1



VDD_NPU



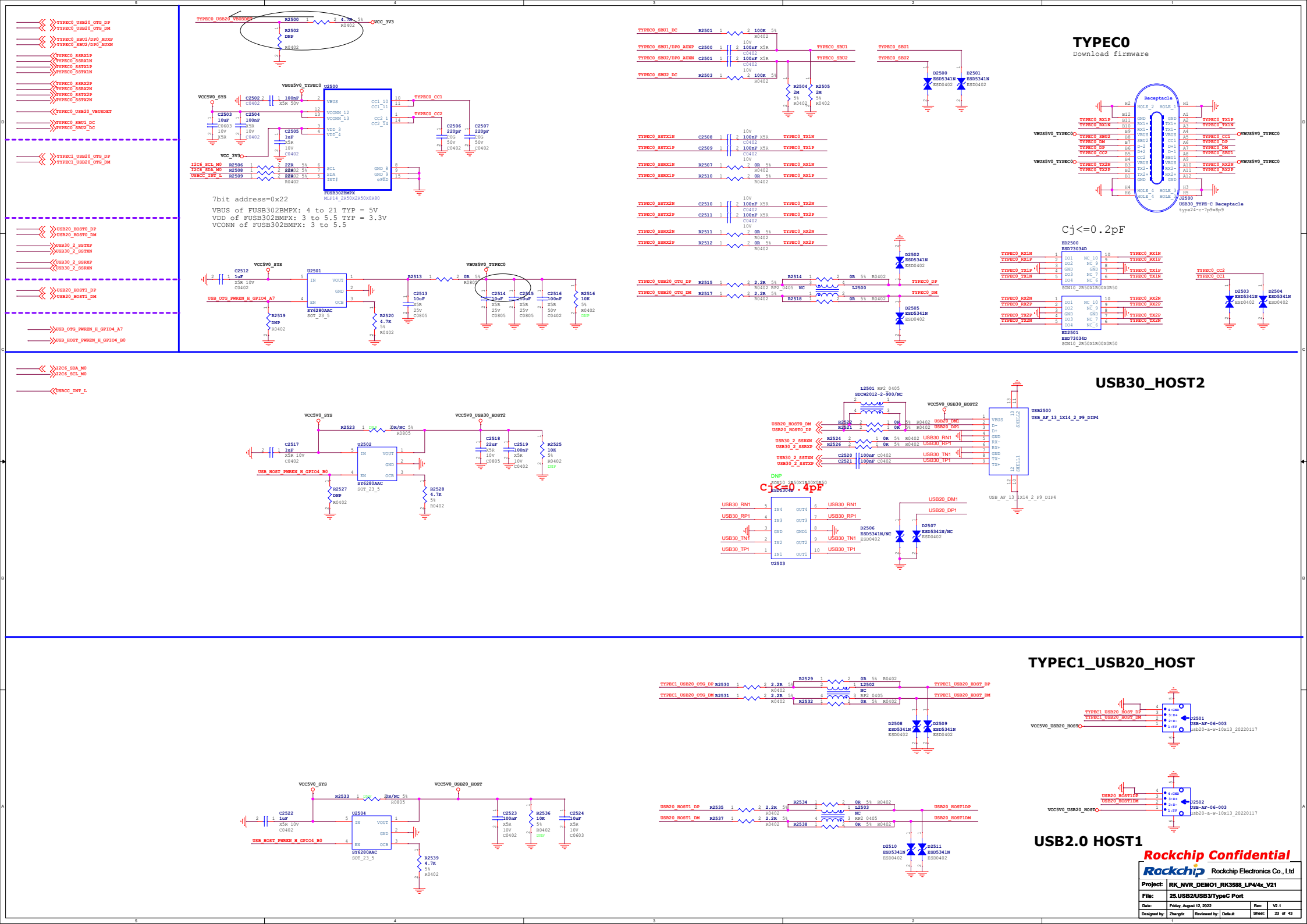
RTC IC



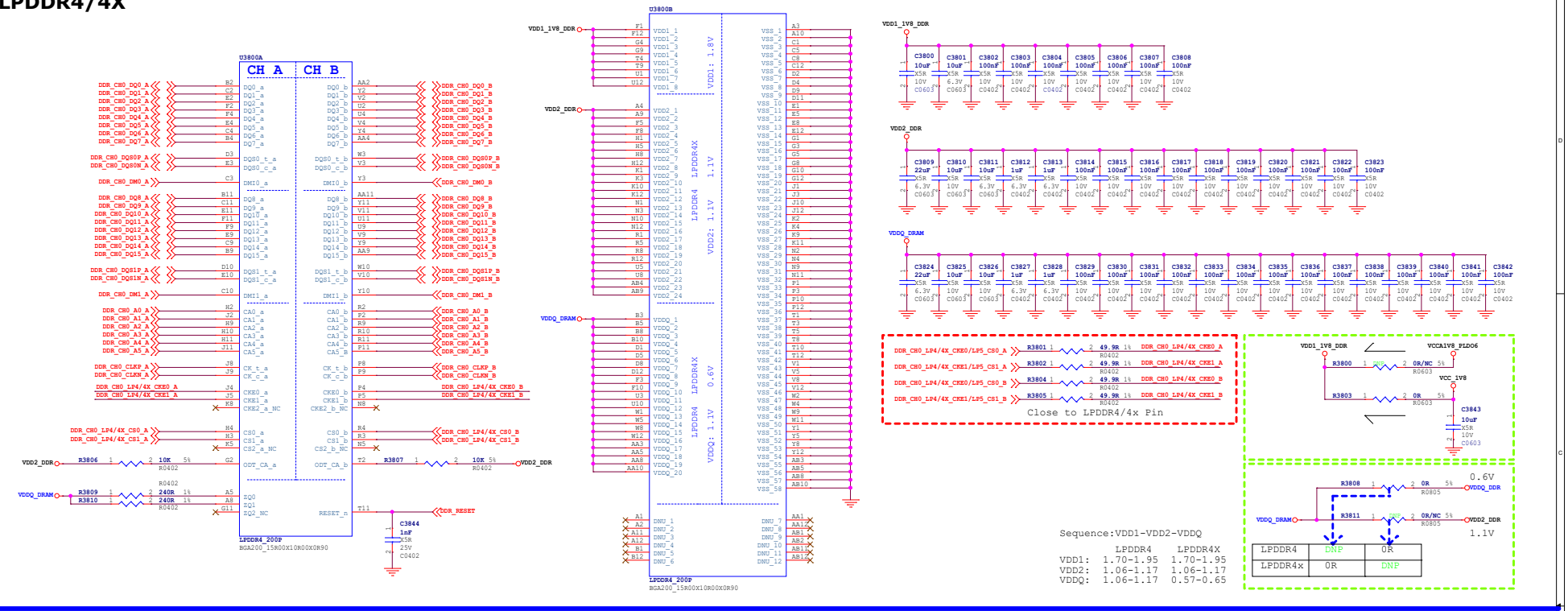
Address:Read A3H,Write A2H

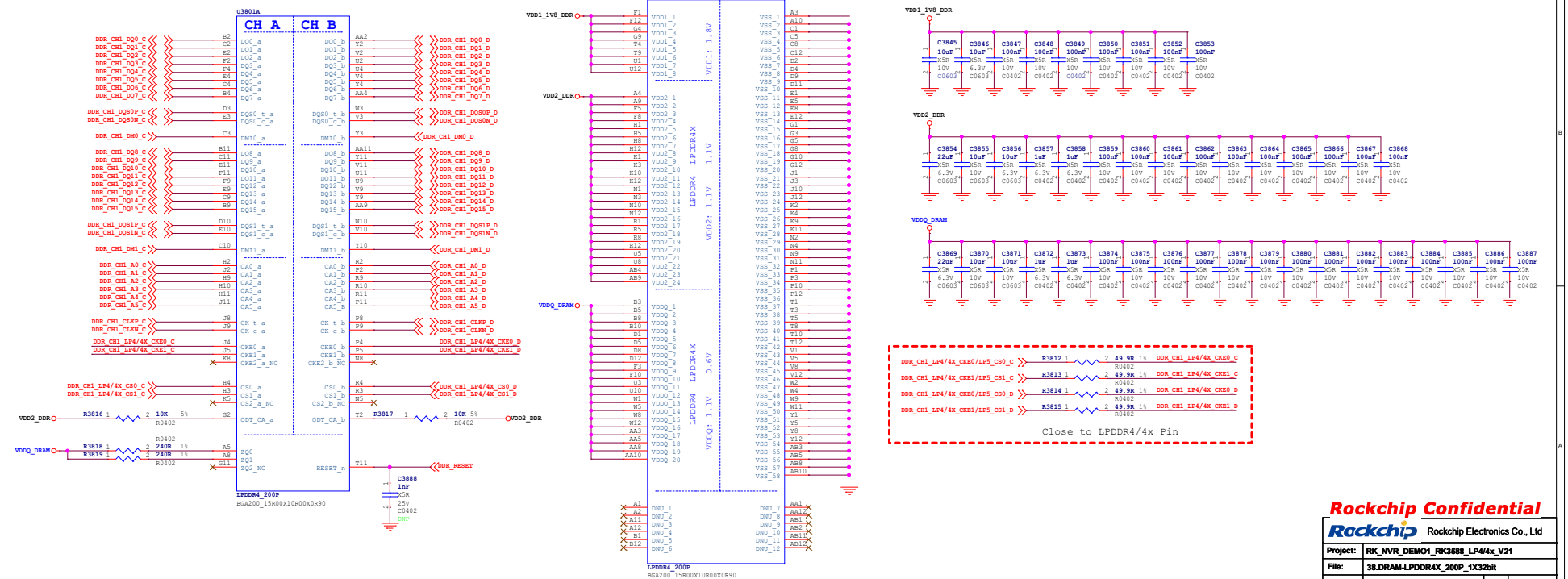
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	23.Power_Ext Discrete/RTC IC				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 43


TYPEC0
Download firmware
USB30_HOST2
TYPEC1_USB20_HOST
USB2.0 HOST1
Cj<=0.2pF
Cj<=0.4pF
7bit address=0x22
VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21
File: 25.USB2/USB3/TypeC Port
Date: Friday, August 12, 2022
Rev: V2.1
Designed by: Zhangtz
Reviewed by: Default
Sheet: 23 of 43

LPDDR4/4X

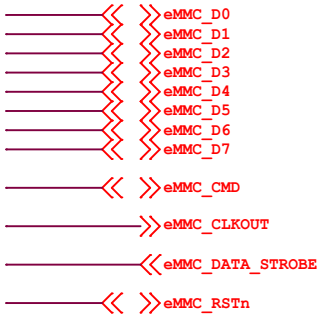


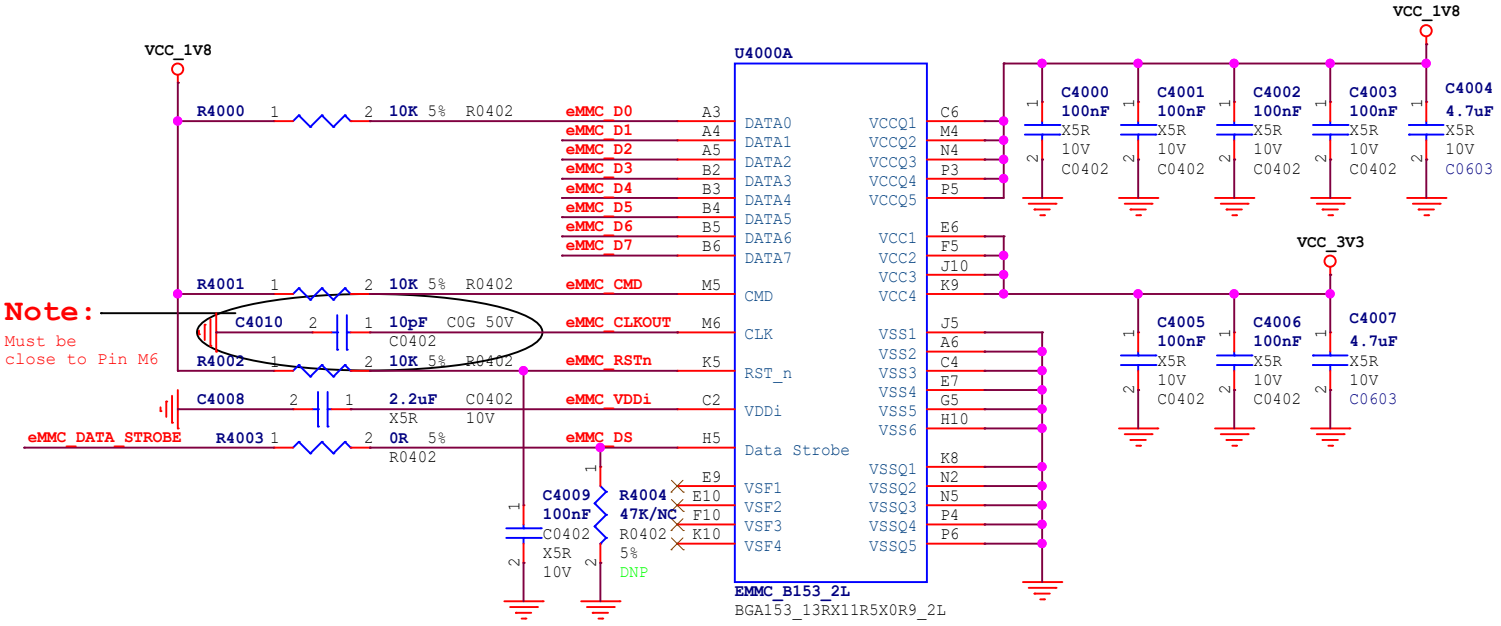


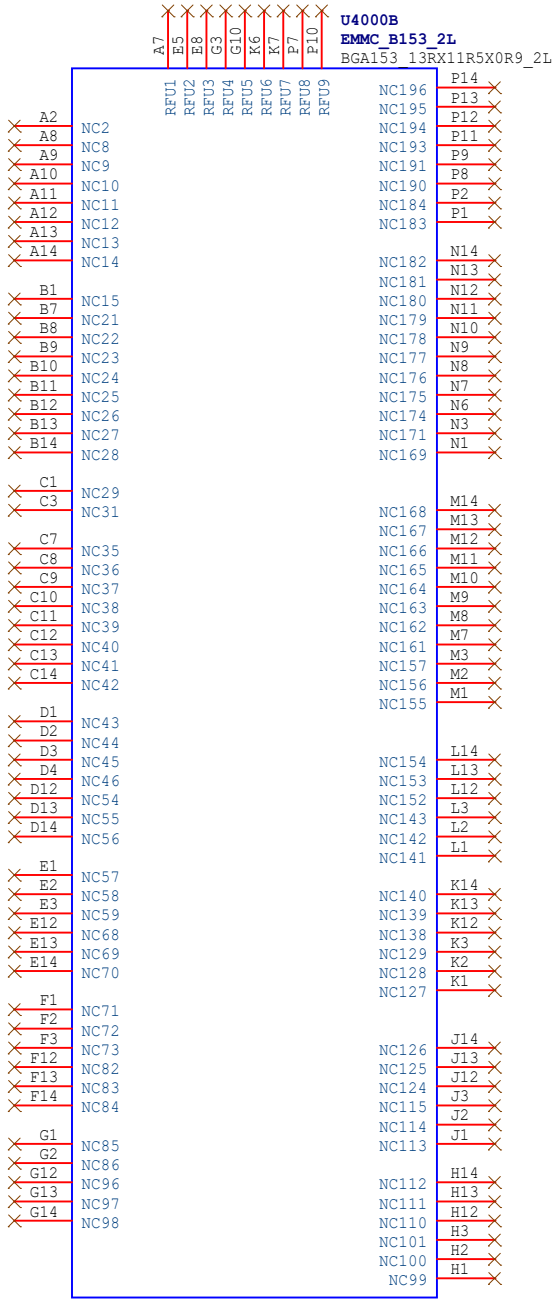
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	38.DRAM-LPDDR4X_200P_1X32bit		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Sheet: 24 of 43

eMMC Flash







Rockchip Confidential

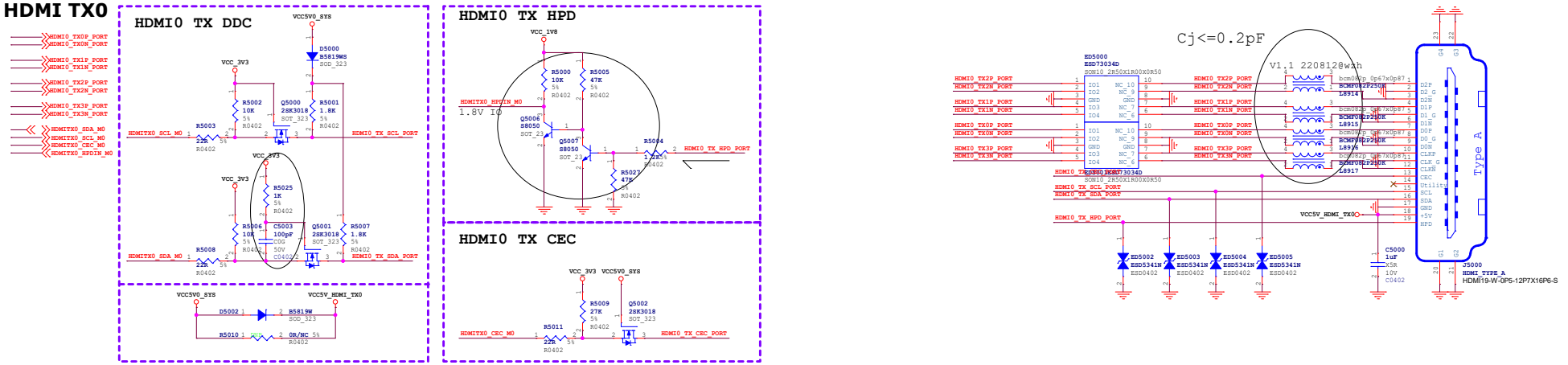
Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	40.Flash-eMMC Flash				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	25 of 43

SPI Flash

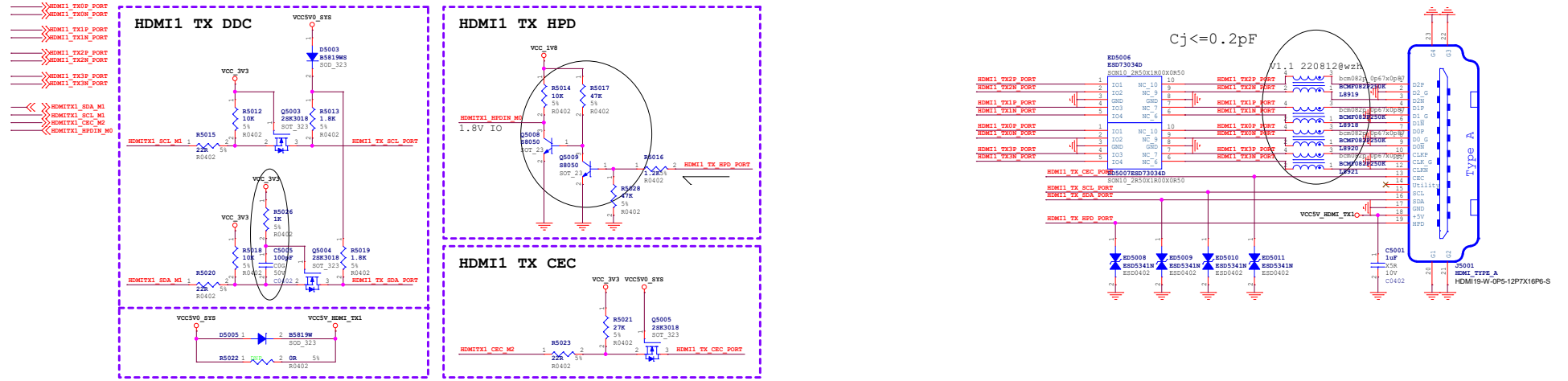
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	43.Flash-SPI FLASH(Option)				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	26 of 43

HDMI TX0

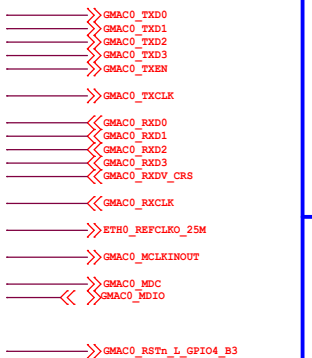


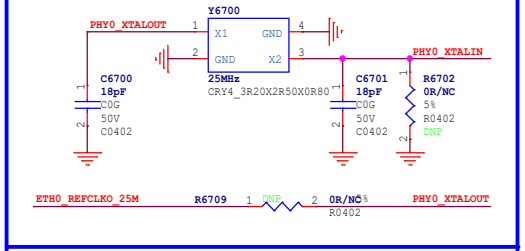
HDMI TX1

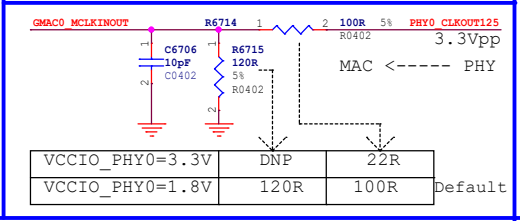


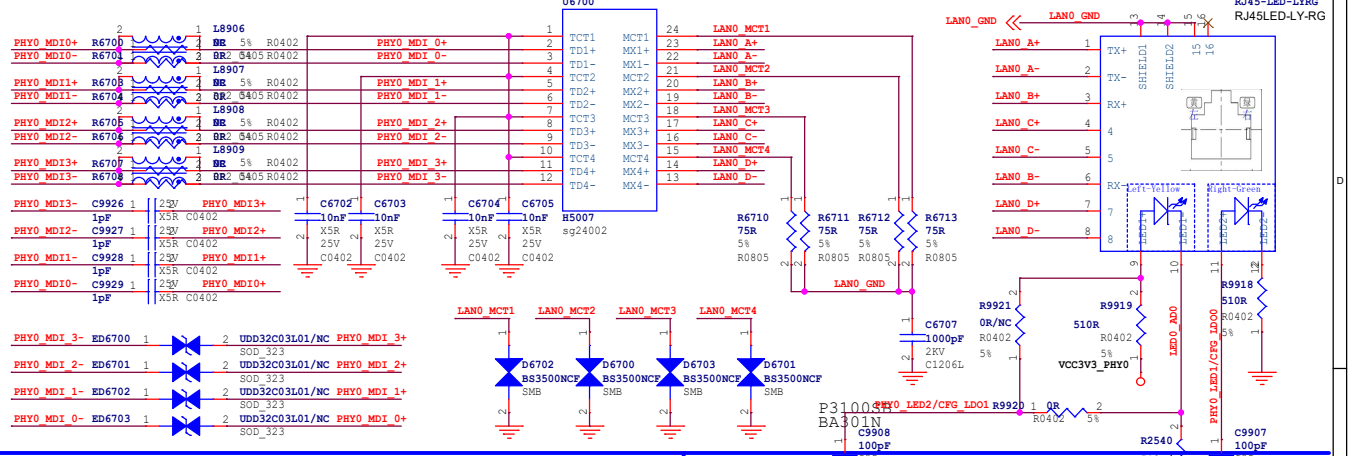
Rockchip Confidential

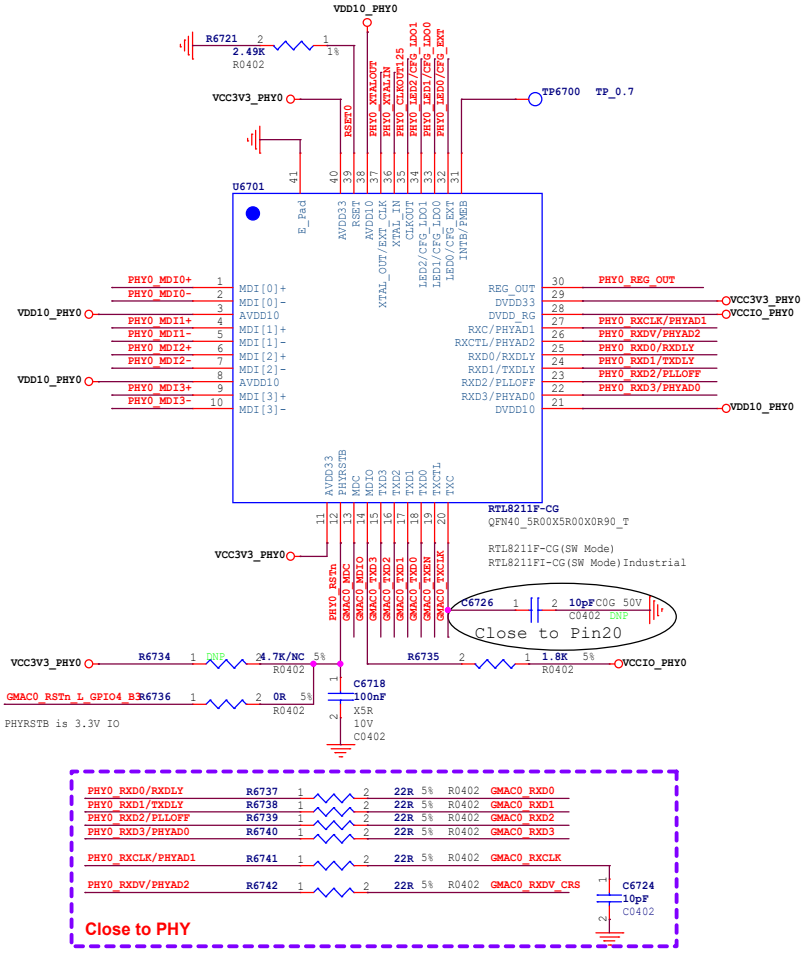
Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	50.VO-HDMI2.1 TX		
Date:	Friday, August 12, 2022	Rev:	V2.1
Designed by:	Zhengtz	Reviewed by:	Sheet: 28 of 43

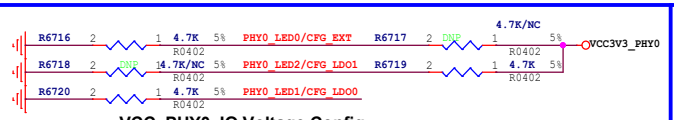




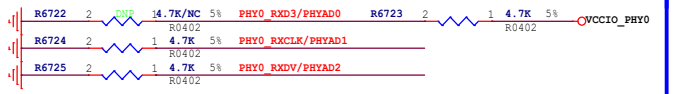






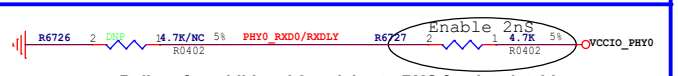


VCC_PHY0_IO Voltage Config



PHY Address Config

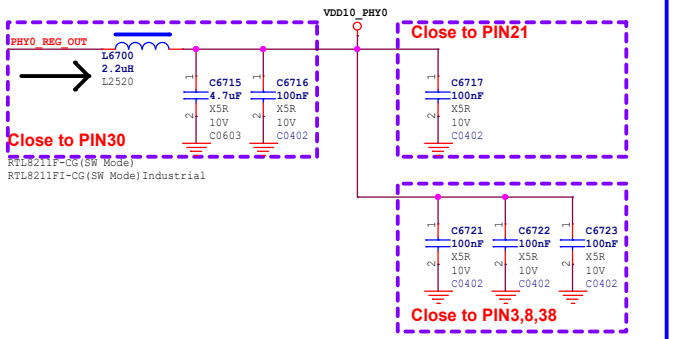
PHY Address	PHYAD[2:0]
1 (default)	3'b001



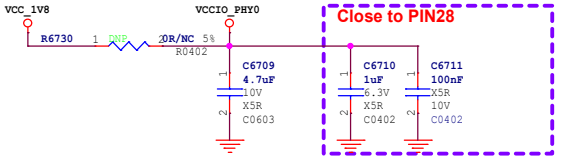
Pull-up for additional 2ns delay to RXC for data latching

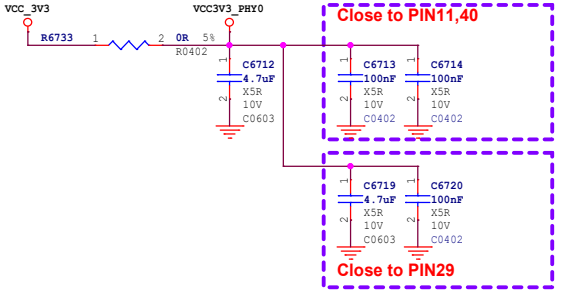
Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode(Low power mode)



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	





Rockchip Confidential

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	67.Ethernet-GEPHY_RGMII0				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	31 of 43

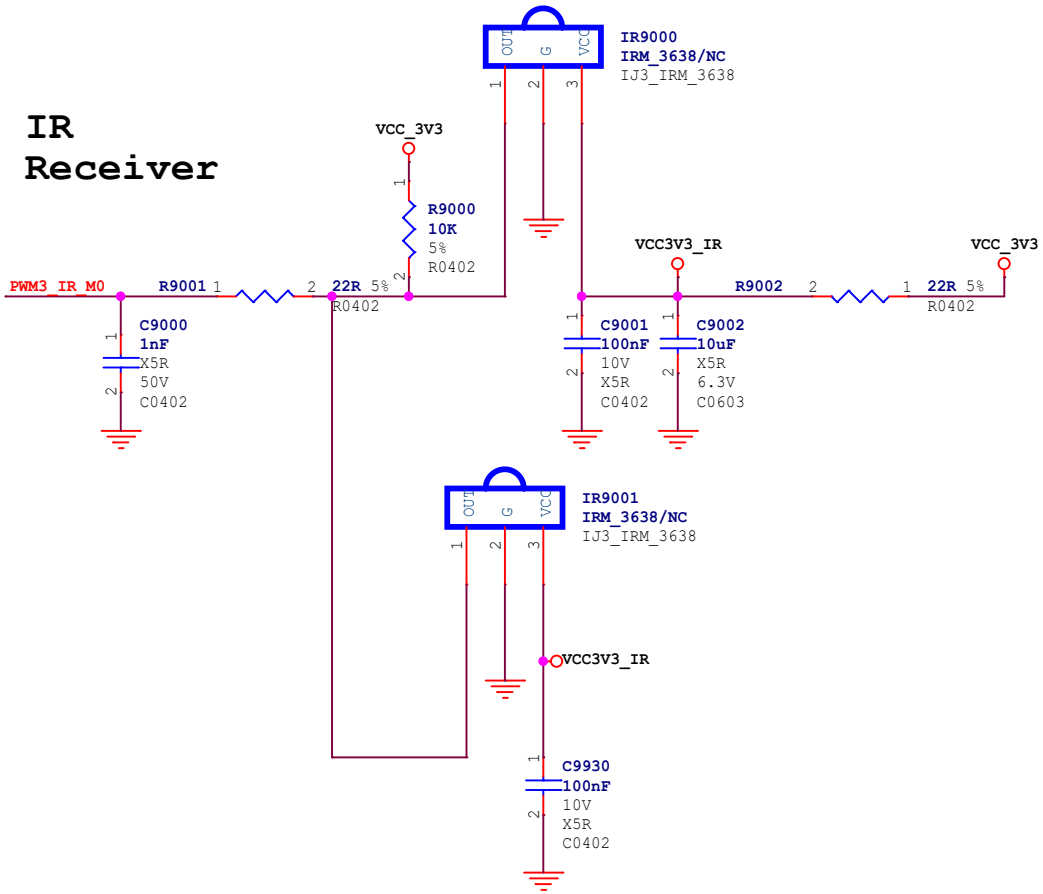
PWM3_IR_M0

Ethernet_LED_EN_H_GPIO3_C0

HDD_LED_EN_H_GPIO3_C1

Power_LED-

IR Receiver



Work_LED

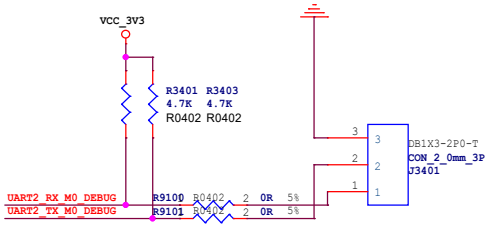
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	90.IR Receiver/LED				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	37 of 43

UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2

Option1



Rockchip Confidential

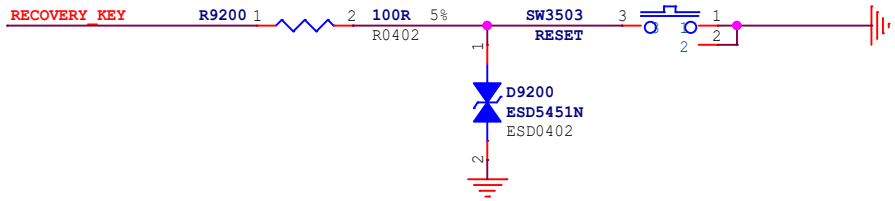
Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	91.Debug UART/JTAG				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	38 of 43

RECOVERY_KEY

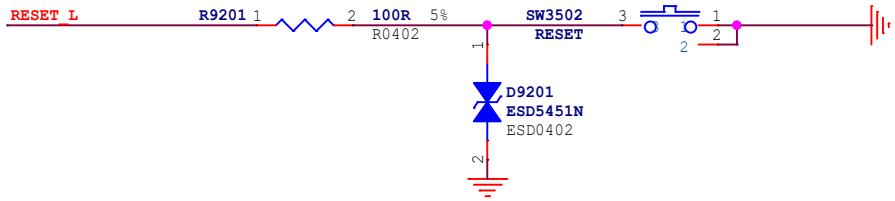
RESET_L

RECOVERY_Key

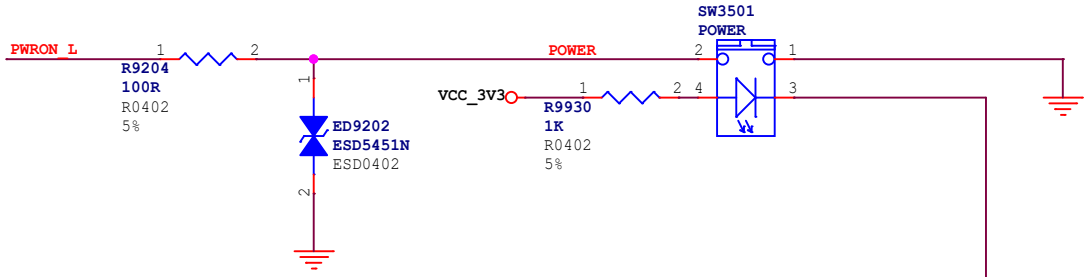
It is recommended to keep the circuit for the actual product update firmware

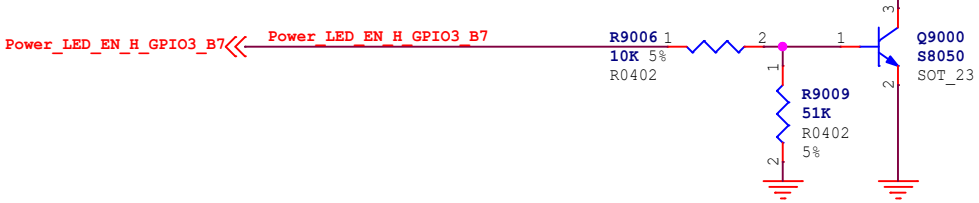


Reset_Key



PWRON_L



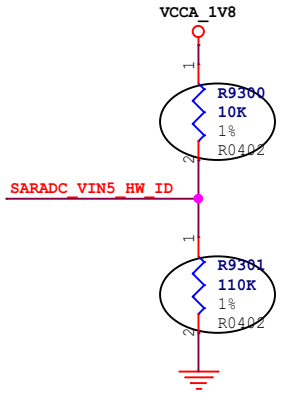


Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	92.KEY				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	39 of 43

SARADC_VIN5_HW_ID

HW_ID



SARADC_VIN1	Up Resistance	Down Resistance	AD value
HW_ID0	10K	DNP	4095
HW_ID1	10K	110K	3754
HW_ID2	20K	100K	3413
HW_ID3	33K	100K	3079
HW_ID4	18K	36K	2730
HW_ID5	36K	51K	2400
HW_ID6	51K	51K	2048
HW_ID7	51K	36K	1695
HW_ID8	36K	18K	1365
HW_ID9	100K	33K	1016
HW_ID10	100K	20K	683
HW_ID11	110K	10K	341
HW_ID12	DNP	10K	0

V10
V21

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	93.HW_ID				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	40 of 43

UART0_TX_M2

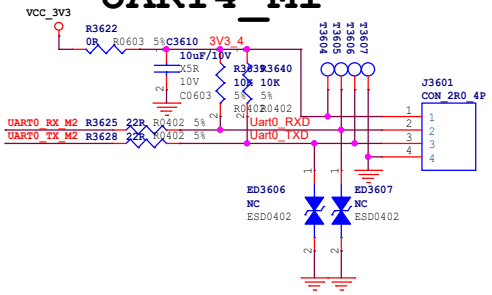
UART0_RX_M2

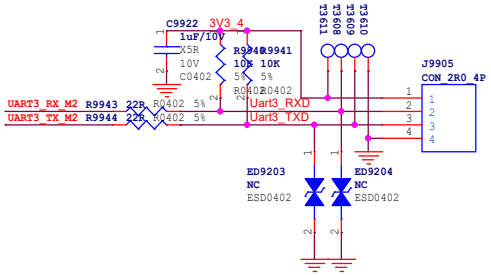
UART3_TX_M2

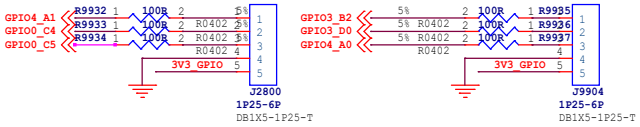
UART3_RX_M2

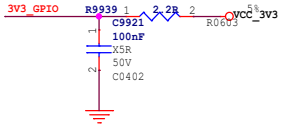
Relay_Ctrl

UART4_M1



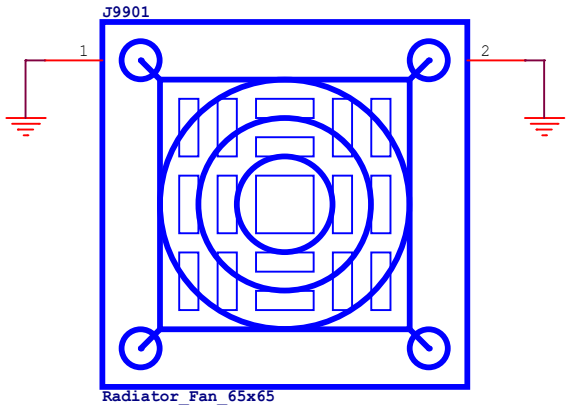




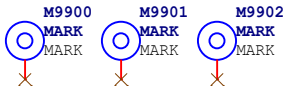


Pin1:DCD,<---,Data Carrier Detect
Pin2:RXD,<---,Receive Data
Pin3:TXD,--->,Transmit Data
Pin4:DTR,--->,Data Terminal Ready
Pin5:COM
Pin6:DSR,<---,Data Set Ready
Pin7:RTS,--->,Request to Send
Pin8:CTS,<---,Clear to Send
Pin9:RI ,<---,Ring Indicator

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	95.RS485/RS232				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	41 of 43



TOP Mark



BOTTOM Mark

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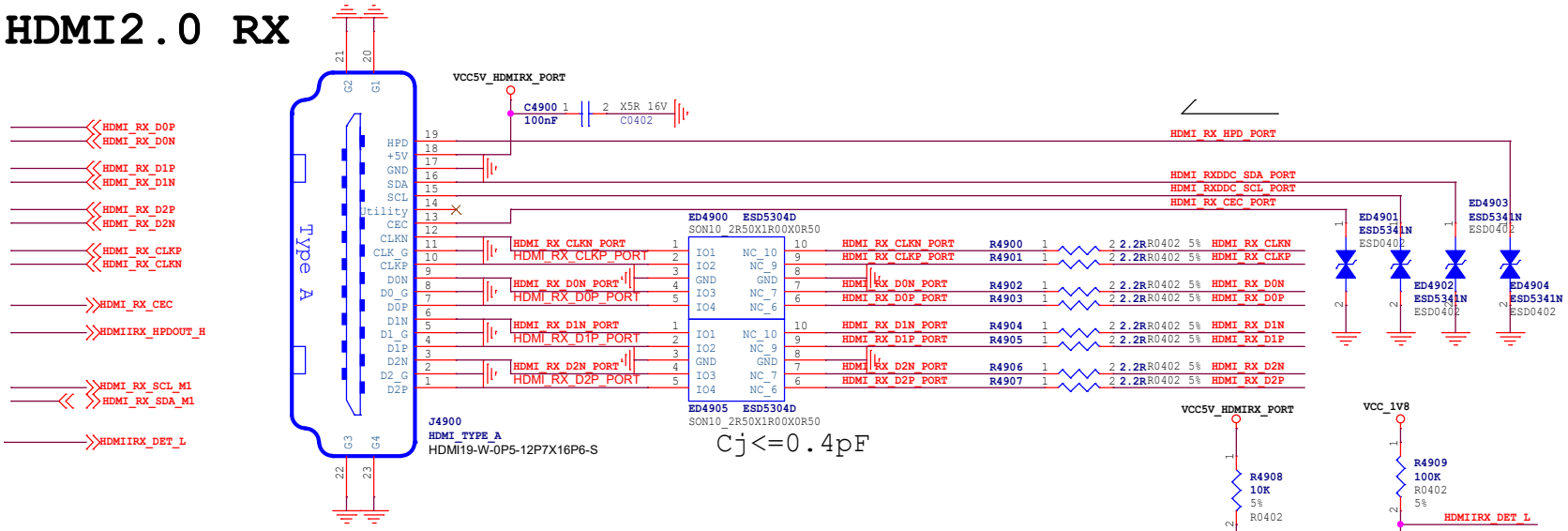
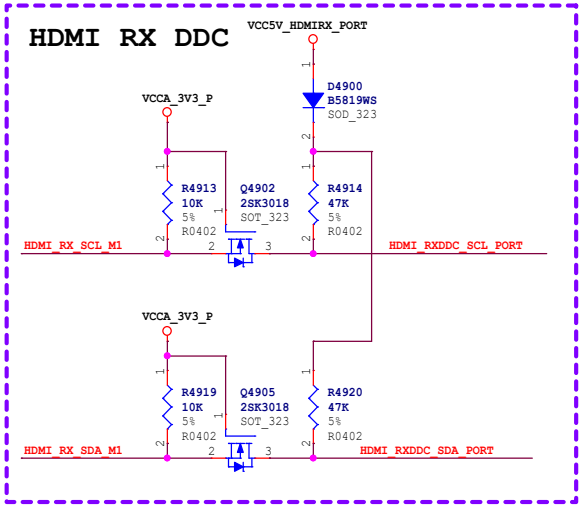
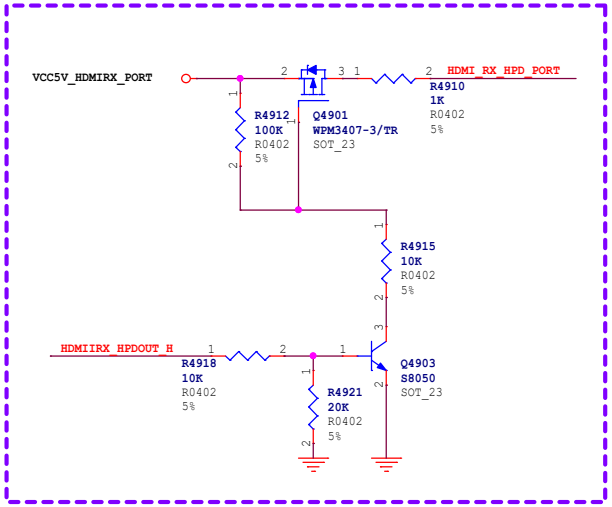
Rockchip Electronics Co., Ltd					
Project:	**RK_NVR_DEMO1_RK3588_LP4/4x_V21**				
File:	**99.Mark/Hole/Heatsink**				
Date:	Friday, August 12, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	43 of 43

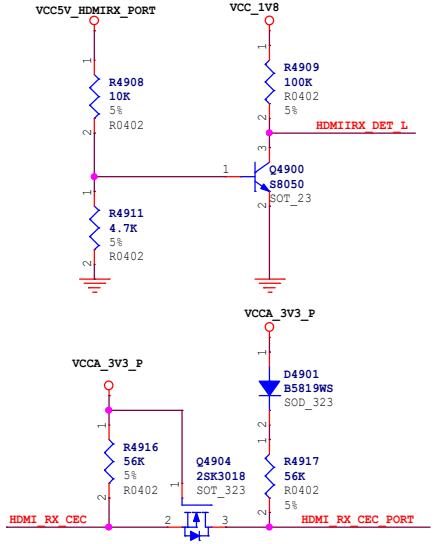
HDMI2.0 RX



HDMI RX DDC



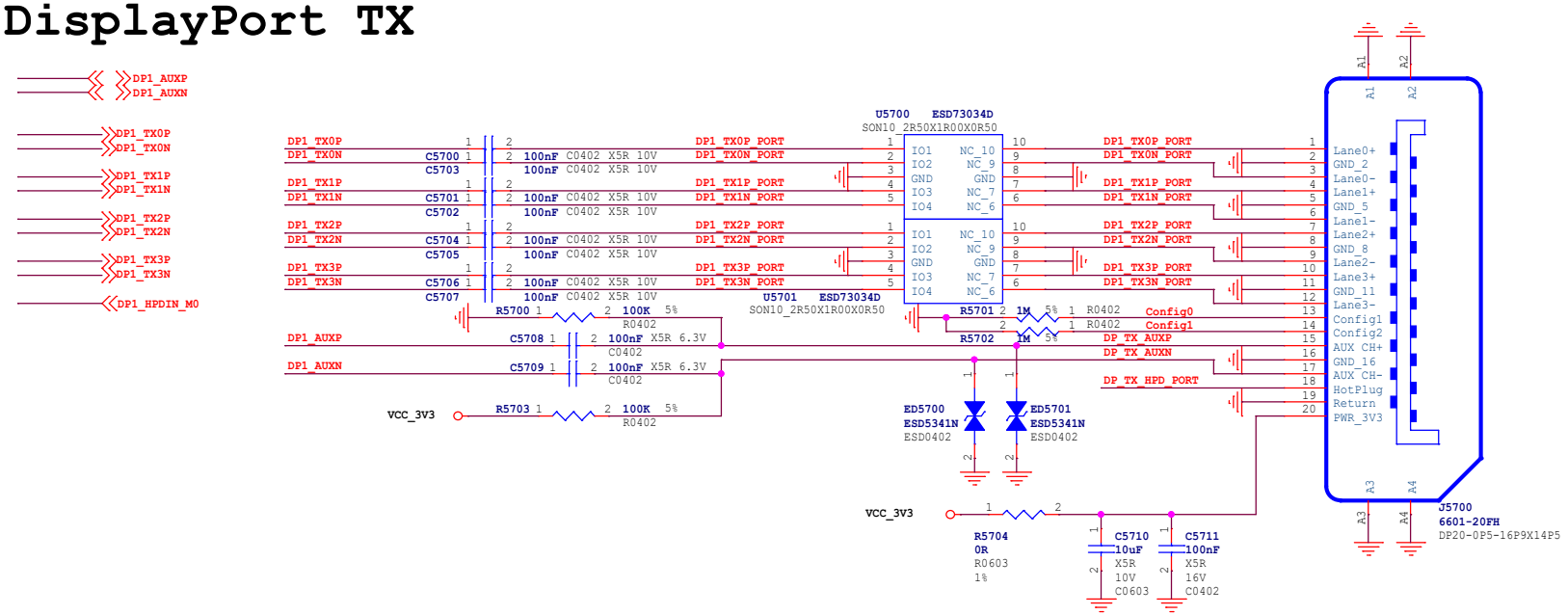




HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V

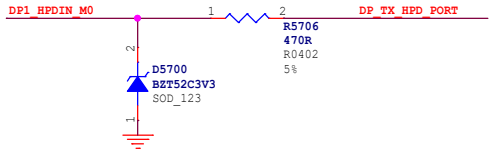
ShenZhen HugSun Technology Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	49.HDMI IN		
Date:	Friday, August 12, 2022	Rev:	V1.0
Designed by:	Wang	Sheet:	51 of 99

DisplayPort TX



DP_TX_HPD

HPD Voltage:2.25-3.6V



ShenZhen HugSun Technology Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	51.DP		
Date:	Friday, August 12, 2022	Rev:	V1.0
Designed by:	Wang	Sheet:	51 of 99

WIFI（802.11 a/b/g/n/ac 2x2 MIMO）