

Schematics Only for RK3588 NVR

RK_NVR_DEMO1_RK3588_LP4XD200P232SD8_V21

Main Functions Introduction

- 1) PMIC: RK806-1+DiscretePower
- 2) RAM: 2 x LPDDR4x 32bit(Option 2 x LPDDR4 32bit)
- 3) ROM: eMMC5.1(Option SPI Nand Falsh)
- 4) Support: 1 x TypeC(With DP TX)
- 5) Support: 1 x USB3.0 HOST + 2 x USB2.0 HOST
- 6) Support: 10 x SATA3.0 Connector (7pin)
- 7) Support: 1 x 4Lanes PCIe Connector
- 8) Support: 2 x HDMI2.1 TX + 1 x HDMI2.0 TX + 1 x HDMI1.4 TX
- 9) Support: 2 x 4Lanes MIPI CSI RX Camera Connector
- 10) Support: 2 x 10/100/1000 Ethernet(RGMII)
- 11) Support: 1 x Line Out, 1 x Line In
- 12) Support: 1 x Buzzer
- 13) Support: 1 x IR Receiver
- 14) Support: 1 x Power LED,1 x Ethernet LED,1 x HDD LED
- 15) Support: 1 x Recovery Key,1x Reset Key
- 16) Support: 1 x RS232
- 17) Support: 1 x RS485
- 18) Support: 1 x UART
- 19) Support: Debug UART(USB to UART),Debug JTAG (4Pin)

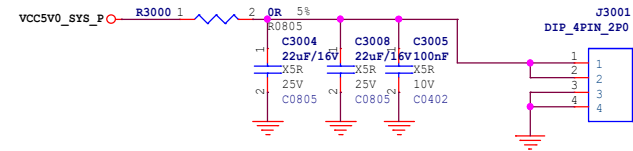
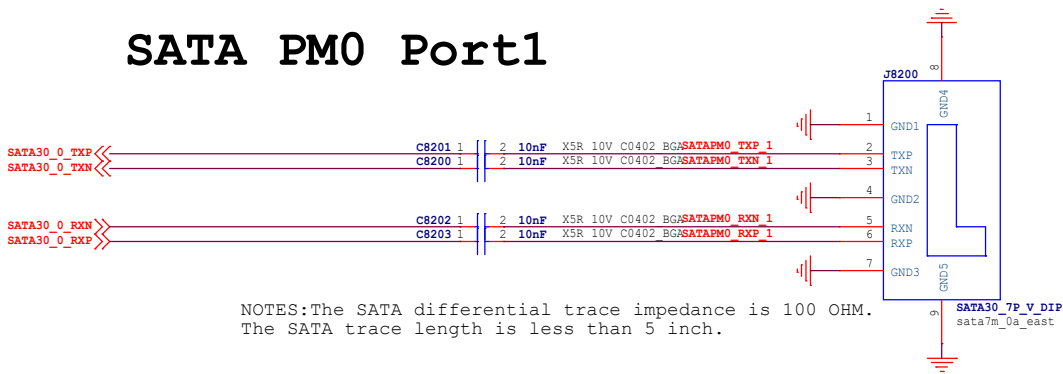
Note:

The RK806 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics. If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

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SATA PM0 Port1



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Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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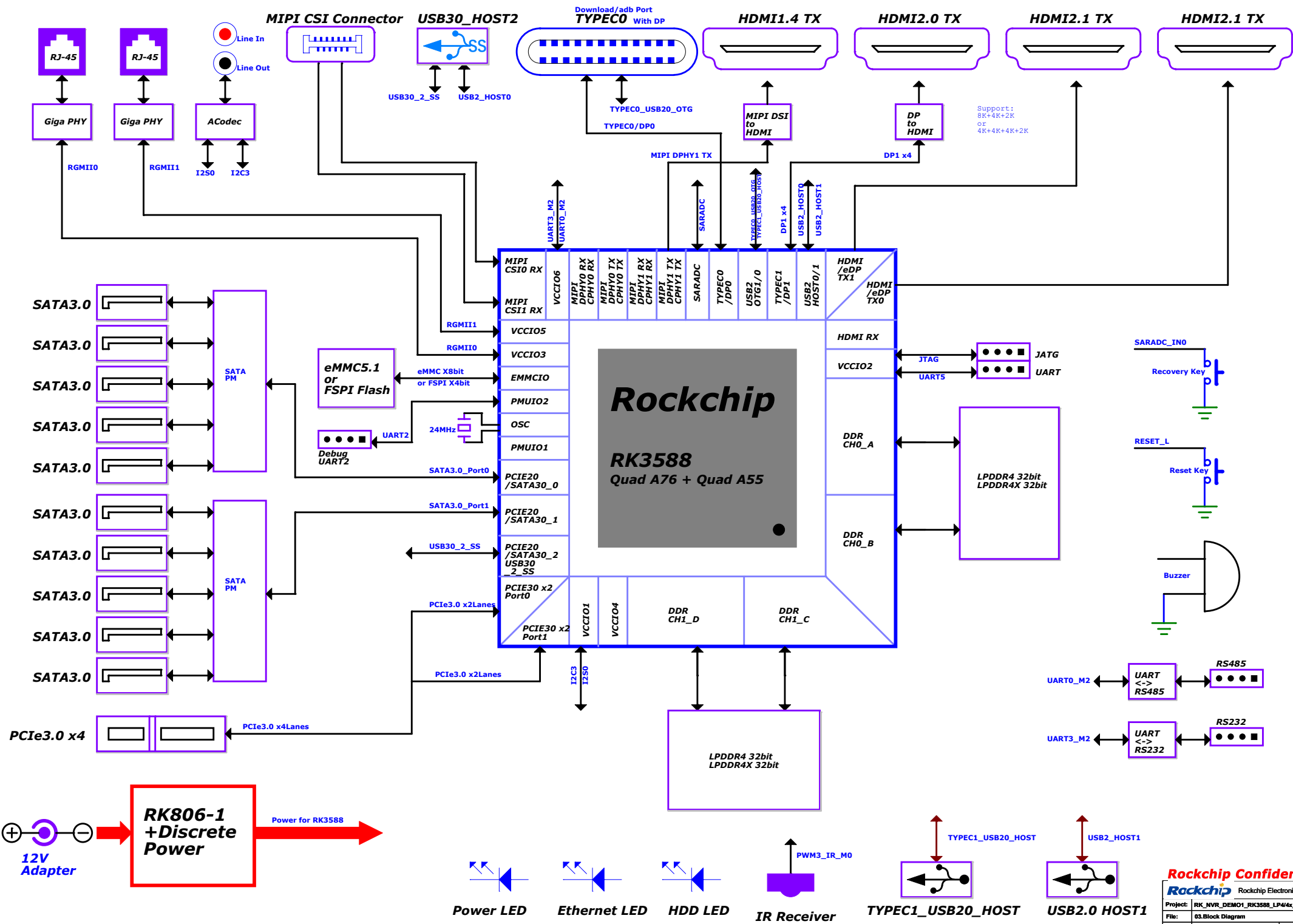
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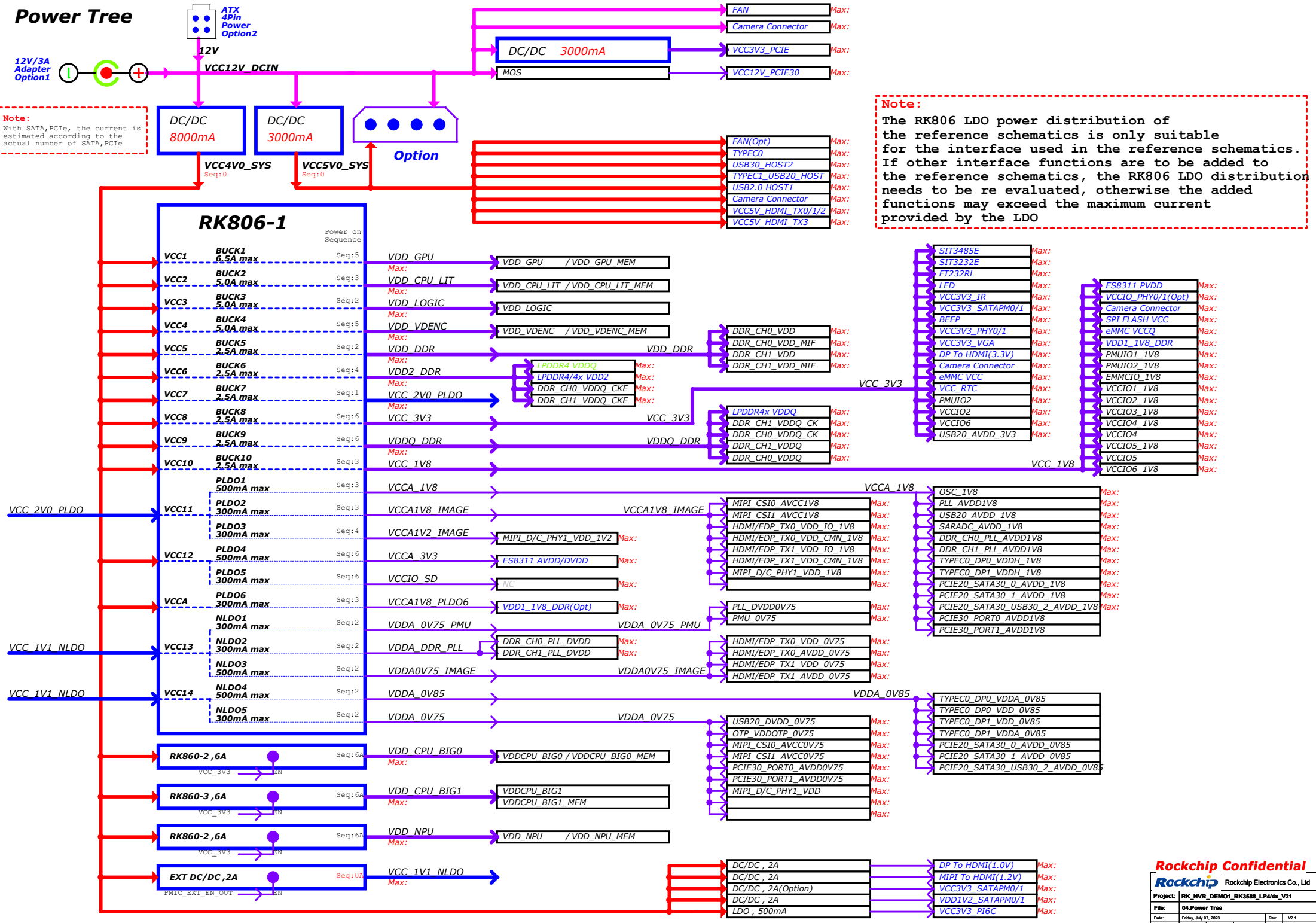
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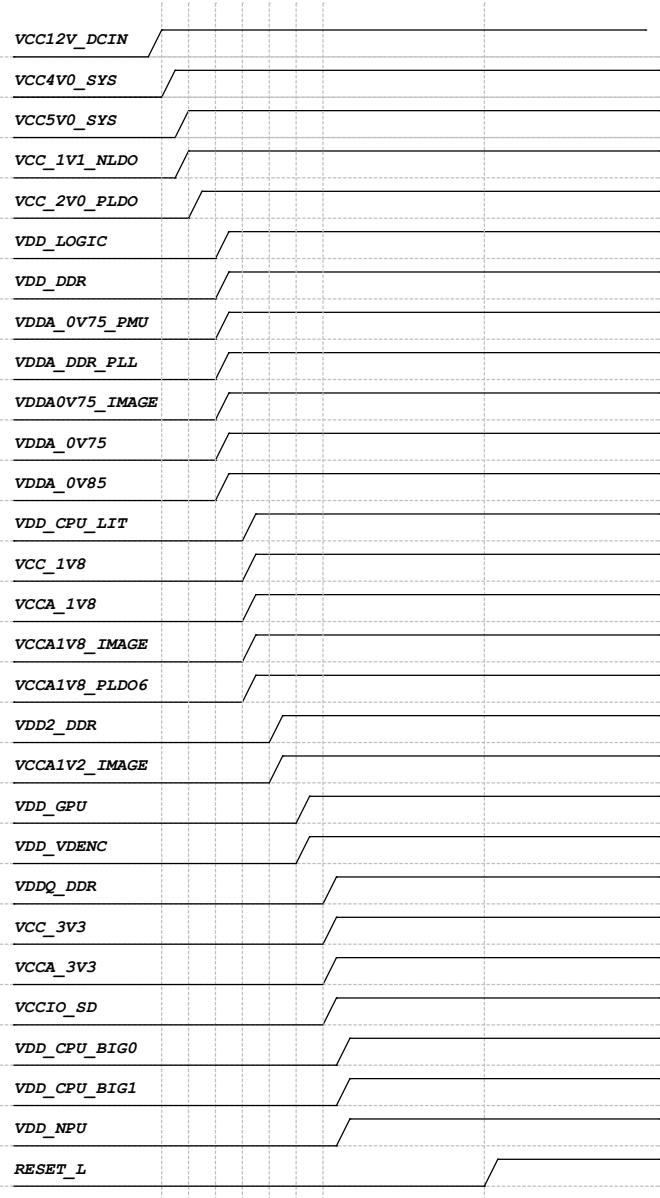
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	5	4	3	2	1
	Revision History				



Power Tree



Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC4V0_SYS	RK806_BUCK1	6.5A	VDD_GPU	Slot:5	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK2	5A	VDD_CPU_LIT	Slot:3	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK3	5A	VDD_LOGIC	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC4V0_SYS	RK806_BUCK4	5A	VDD_VDENC	Slot:5	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK5	2.5A	VDD_DDR	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK6	2.5A	VDD2_DDR	Slot:4	ADJ FB=0.5V 2.0V	ON	1.1V LPDDR4/4x 2.0V	TBD	TBD
VCC4V0_SYS	RK806_BUCK7	2.5A	VCC_2V0_PLDO	Slot:1	2.0V	ON	2.0V	TBD	TBD
VCC4V0_SYS	RK806_BUCK8	2.5A	VCC_3V3	Slot:6	3.3V	ON	3.3V	TBD	TBD
VCC4V0_SYS	RK806_BUCK9	2.5A	VDDQ_DDR	Slot:6	ADJ FB=0.5V 1.8V	ON	0.6V LPDDR4/4x 1.8V	TBD	TBD
VCC4V0_SYS	RK806_BUCK10	2.5A	VCC_1V8	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_IMAGE	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VCCA1V2_IMAGE	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC4V0_SYS	RK806_PLDO4	0.5A	VCCA_3V3	Slot:6	3.3V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD	Slot:6	3.3V	ON	3.3V	TBD	TBD
VCC4V0_SYS	RK806_PLDO6	0.3A	VCCA1V8_PLDO6	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDDA_0V75_PMU	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_IMAGE	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETh								
VCC12V_DCIN	EXT BUCK	8A	VCC4V0_SYS	Slot:0	4.0V	ON	4.0V	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO	Slot:0A	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_SYS	Slot:0A	5.2V	ON	5.2V	TBD	TBD
VCC4V0_SYS	RK860-2	6A	VDD_CPU_BIG0	Slot:6A	0.8V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK860-3	6A	VDD_CPU_BIG1	Slot:6A	0.8V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK860-2	6A	VDD_NPU	Slot:6A	0.8V	ON	DVFS	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8 VCC_3V3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8	1.8V
VCCIO1	Pin G20	1.8V Only	VDDIO1_1V8	VCC_1V8	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VDDIO2_1V8 VCCIO2	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin Y26	1.8V Only	VDDIO3_1V8	VCC_1V8	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VDDIO4_1V8 VCCIO4	VCC_1V8 VCC_1V8	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VDDIO5_1V8 VCCIO5	VCC_1V8 VCC_3V3	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VDDIO6_1V8 VCCIO6	VCC_1V8 VCC_3V3	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

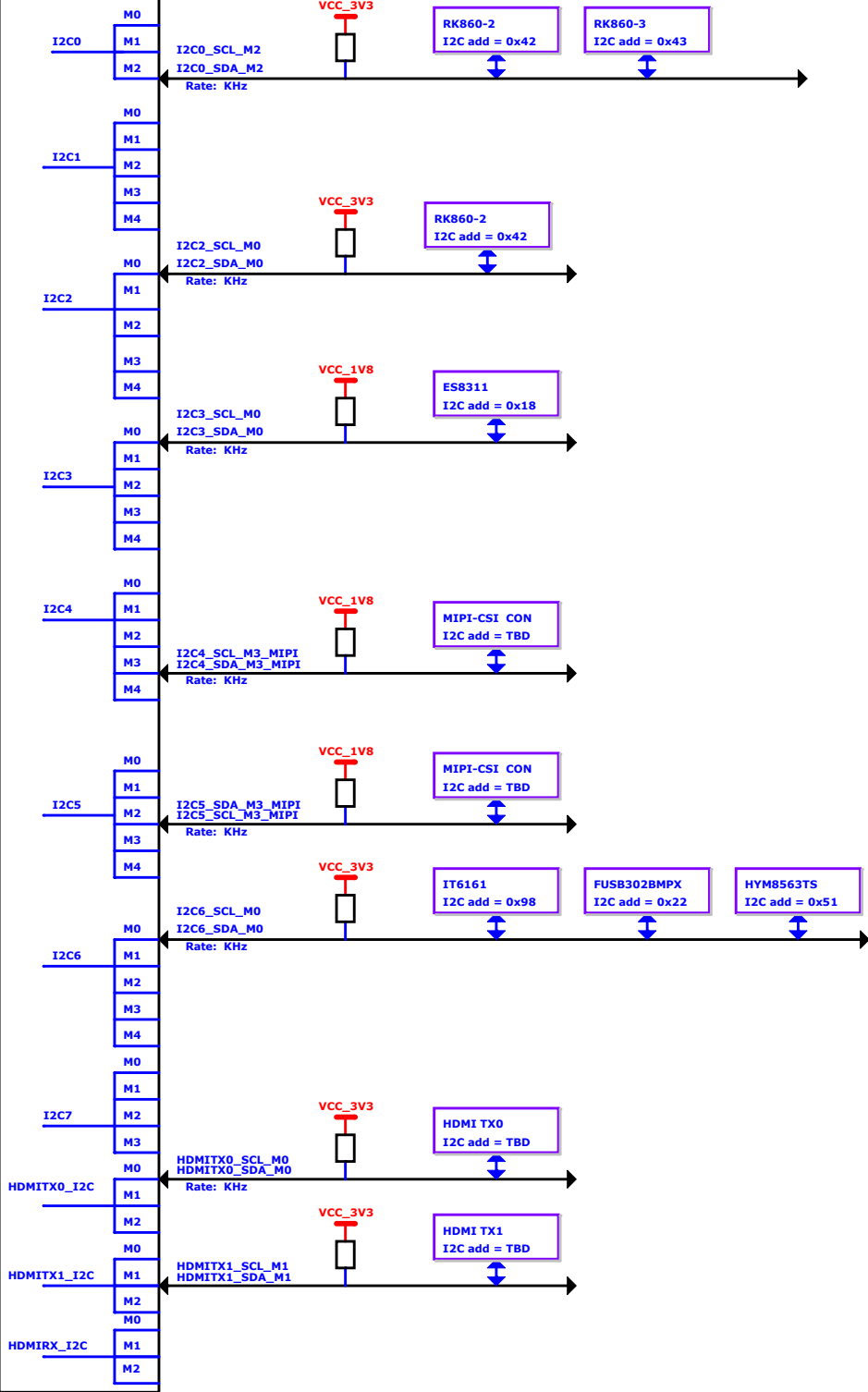
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Rackchip Rackchip Electronics Co., Ltd

Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	05.Power Sequence/IO Domain Map		
Date:	Friday, July 07, 2023	Rev:	V2.1
Designed by:	Zhangtz	Reviewed by:	Default
Sheet:	6	of	43

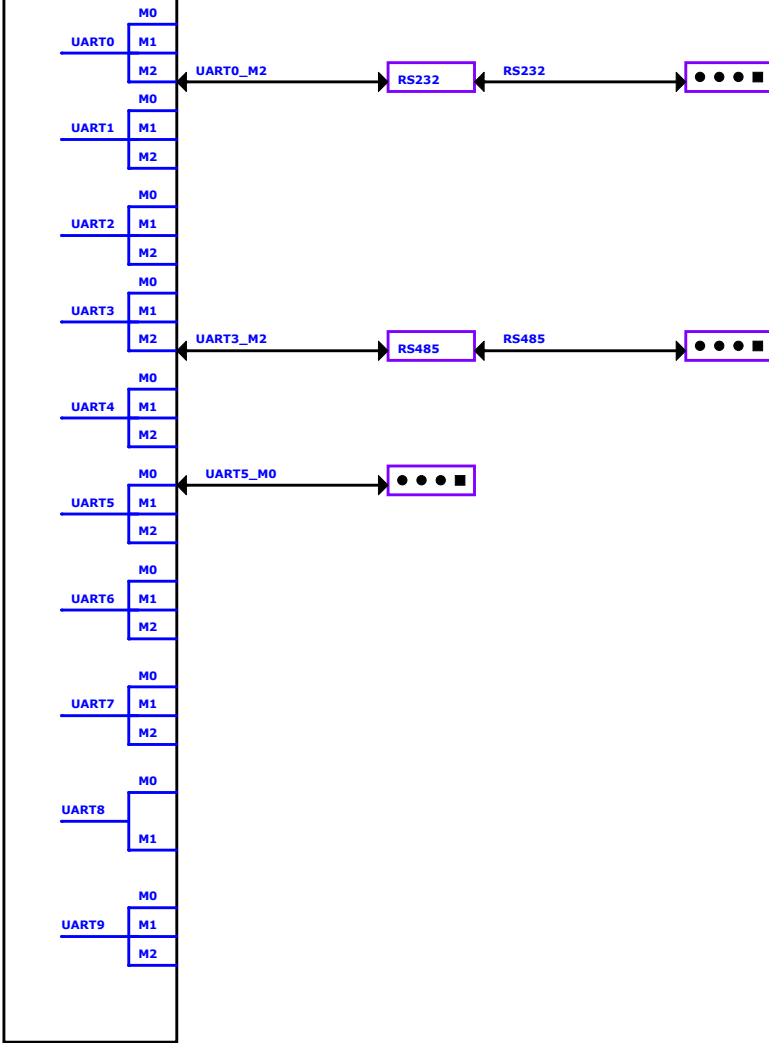
I2C MAP

RK3588



UART MAP

RK3588

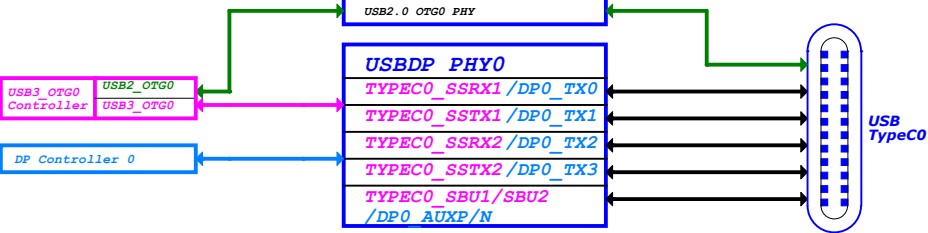


USB Controller Configure Table

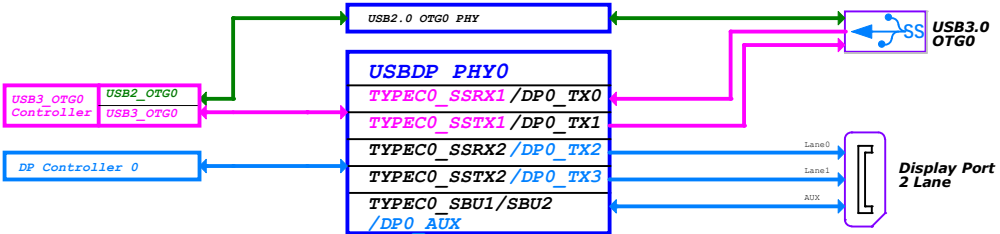
Controller Name	Pin Name	Type-C Function	Dp5Lane Function		USB30 OTG+Dp5Lane Function		USB20 OTG+Dp5Lane Function		USB20 OTG+Dp4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TPP0C0_0M01_DP_A0SDP	TPP0C0_0M01	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP
	TPP0C0_0M01_DP_A0SDN	TPP0C0_0M01	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN
	TPP0C0_0M01P_TXD0	TPP0C0_0M01P	DPO_TX0P	DPO_TX0P	TPP0C0_0M01P_TXD0	DPO_TX0P	DPO_TX0P	DPO_TX0P	DPO_TX0P	DPO_TX0P
	TPP0C0_0M01P_TXD0N	TPP0C0_0M01P	DPO_TX0N	DPO_TX0N	TPP0C0_0M01P_TXD0N	DPO_TX0N	DPO_TX0N	DPO_TX0N	DPO_TX0N	DPO_TX0N
	TPP0C0_0M01P_TXD1	TPP0C0_0M01P	DPO_TX1P	DPO_TX1P	TPP0C0_0M01P_TXD1	DPO_TX1P	DPO_TX1P	DPO_TX1P	DPO_TX1P	DPO_TX1P
	TPP0C0_0M01P_TXD1N	TPP0C0_0M01P	DPO_TX1N	DPO_TX1N	TPP0C0_0M01P_TXD1N	DPO_TX1N	DPO_TX1N	DPO_TX1N	DPO_TX1N	DPO_TX1N
USB30 OTG0 Device or Host	TPP0C0_0M01P_TXD2	TPP0C0_0M01P	DPO_TX2P	DPO_TX2P	TPP0C0_0M01P_TXD2	DPO_TX2P	DPO_TX2P	DPO_TX2P	DPO_TX2P	DPO_TX2P
	TPP0C0_0M01P_TXD2N	TPP0C0_0M01P	DPO_TX2N	DPO_TX2N	TPP0C0_0M01P_TXD2N	DPO_TX2N	DPO_TX2N	DPO_TX2N	DPO_TX2N	DPO_TX2N
	TPP0C0_0M01P_TXD3	TPP0C0_0M01P	DPO_TX3P	DPO_TX3P	TPP0C0_0M01P_TXD3	DPO_TX3P	DPO_TX3P	DPO_TX3P	DPO_TX3P	DPO_TX3P
	TPP0C0_0M01P_TXD3N	TPP0C0_0M01P	DPO_TX3N	DPO_TX3N	TPP0C0_0M01P_TXD3N	DPO_TX3N	DPO_TX3N	DPO_TX3N	DPO_TX3N	DPO_TX3N
	TPP0C0_0M01P_TXD4	TPP0C0_0M01P	DPO_TX4P	DPO_TX4P	TPP0C0_0M01P_TXD4	DPO_TX4P	DPO_TX4P	DPO_TX4P	DPO_TX4P	DPO_TX4P
	TPP0C0_0M01P_TXD4N	TPP0C0_0M01P	DPO_TX4N	DPO_TX4N	TPP0C0_0M01P_TXD4N	DPO_TX4N	DPO_TX4N	DPO_TX4N	DPO_TX4N	DPO_TX4N
USB30 OTG1 Device or Host	TPP0C1_0M02_DP_A0SDP	TPP0C1_0M02	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP	DPO_A0SDP
	TPP0C1_0M02_DP_A0SDN	TPP0C1_0M02	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN	DPO_A0SDN
	TPP0C1_0M02P_TXD0	TPP0C1_0M02P	DPO_TX0P	DPO_TX0P	TPP0C1_0M02P_TXD0	DPO_TX0P	DPO_TX0P	DPO_TX0P	DPO_TX0P	DPO_TX0P
	TPP0C1_0M02P_TXD0N	TPP0C1_0M02P	DPO_TX0N	DPO_TX0N	TPP0C1_0M02P_TXD0N	DPO_TX0N	DPO_TX0N	DPO_TX0N	DPO_TX0N	DPO_TX0N
	TPP0C1_0M02P_TXD1	TPP0C1_0M02P	DPO_TX1P	DPO_TX1P	TPP0C1_0M02P_TXD1	DPO_TX1P	DPO_TX1P	DPO_TX1P	DPO_TX1P	DPO_TX1P
	TPP0C1_0M02P_TXD1N	TPP0C1_0M02P	DPO_TX1N	DPO_TX1N	TPP0C1_0M02P_TXD1N	DPO_TX1N	DPO_TX1N	DPO_TX1N	DPO_TX1N	DPO_TX1N
USB30 OTG1 Device or Host	TPP0C1_0M02P_TXD2	TPP0C1_0M02P	DPO_TX2P	DPO_TX2P	TPP0C1_0M02P_TXD2	DPO_TX2P	DPO_TX2P	DPO_TX2P	DPO_TX2P	DPO_TX2P
	TPP0C1_0M02P_TXD2N	TPP0C1_0M02P	DPO_TX2N	DPO_TX2N	TPP0C1_0M02P_TXD2N	DPO_TX2N	DPO_TX2N	DPO_TX2N	DPO_TX2N	DPO_TX2N
	TPP0C1_0M02P_TXD3	TPP0C1_0M02P	DPO_TX3P	DPO_TX3P	TPP0C1_0M02P_TXD3	DPO_TX3P	DPO_TX3P	DPO_TX3P	DPO_TX3P	DPO_TX3P
	TPP0C1_0M02P_TXD3N	TPP0C1_0M02P	DPO_TX3N	DPO_TX3N	TPP0C1_0M02P_TXD3N	DPO_TX3N	DPO_TX3N	DPO_TX3N	DPO_TX3N	DPO_TX3N
	TPP0C1_0M02P_TXD4	TPP0C1_0M02P	DPO_TX4P	DPO_TX4P	TPP0C1_0M02P_TXD4	DPO_TX4P	DPO_TX4P	DPO_TX4P	DPO_TX4P	DPO_TX4P
	TPP0C1_0M02P_TXD4N	TPP0C1_0M02P	DPO_TX4N	DPO_TX4N	TPP0C1_0M02P_TXD4N	DPO_TX4N	DPO_TX4N	DPO_TX4N	DPO_TX4N	DPO_TX4N
USB20 OTG0 Device or Host	TPP0C0_0M01P_DP_A0SDP	TPP0C0_0M01P	DPO_A0SDP	DPO_A0SDP	TPP0C0_0M01P_DP_A0SDP	DPO_A0SDP	DPO_A0SDP	TPP0C0_0M01P_DP_A0SDP	DPO_A0SDP	DPO_A0SDP
	TPP0C0_0M01P_DP_A0SDN	TPP0C0_0M01P	DPO_A0SDN	DPO_A0SDN	TPP0C0_0M01P_DP_A0SDN	DPO_A0SDN	DPO_A0SDN	TPP0C0_0M01P_DP_A0SDN	DPO_A0SDN	DPO_A0SDN
USB30 HOST	PCIE0_1_RXD/SARX0_2_TXD/USB0_1_OTGDP		OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
	PCIE0_1_RXD/SARX0_2_TXD/USB0_1_OTGDP		USB30 HOST	USB30 HOST	USB30 HOST	USB30 HOST	USB30 HOST	USB30 HOST	USB30 HOST	USB30 HOST
	PCIE0_1_RXD/SARX0_2_TXD/USB0_1_OTGDP		USB30_1_OTGDP	USB30_2_OTGDP	USB30_1_OTGDP	USB30_2_OTGDP	USB30_1_OTGDP	USB30_2_OTGDP	USB30_1_OTGDP	USB30_2_OTGDP
	PCIE0_1_RXD/SARX0_2_TXD/USB0_1_OTGDP		USB30_1_OTGDP	USB30_2_OTGDP	USB30_1_OTGDP	USB30_2_OTGDP	USB30_1_OTGDP	USB30_2_OTGDP	USB30_1_OTGDP	USB30_2_OTGDP
USB30 HOST2										
USB30 HOST0	USB0_HOST0_DP		USB0_HOST0_DP	USB0_HOST0_DP						
	USB0_HOST0_DP		USB0_HOST0_DP	USB0_HOST0_DP						
USB30 HOST1	USB0_HOST1_DP		USB0_HOST1_DP	USB0_HOST1_DP						
	USB0_HOST1_DP		USB0_HOST1_DP	USB0_HOST1_DP						
					TPP0C0_0M01P_DP_A0SDP	TPP0C0_0M01P_DP_A0SDP				
					TPP0C0_0M01P_DP_A0SDP	TPP0C0_0M01P_DP_A0SDP				

Note:
0: Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1: Lane0/1/2/3 TxData mapping to Lane0/1/0/1_TXDP/N

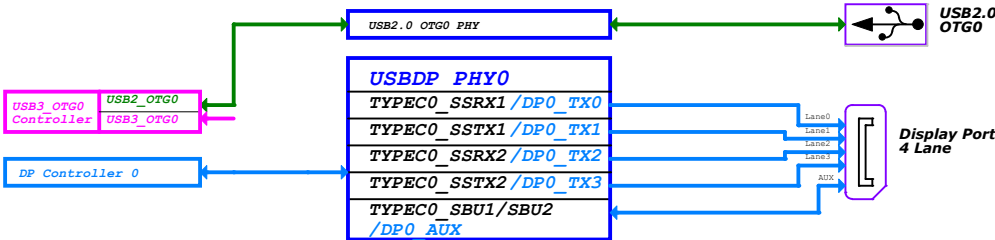
Config0:
TypeC0 (With DP function)



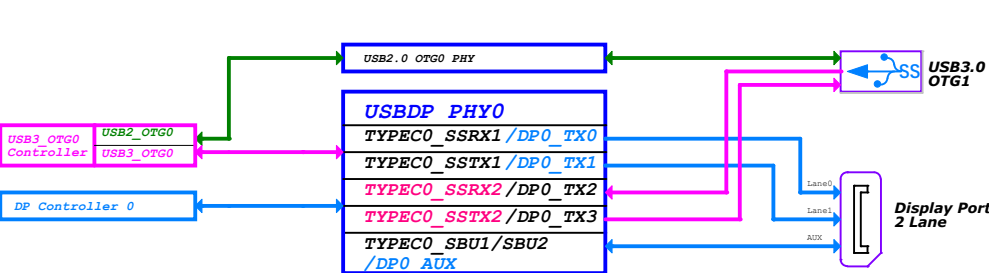
Config3:
USB3.0 OTG0 + DP0 2Lane(Swap ON)



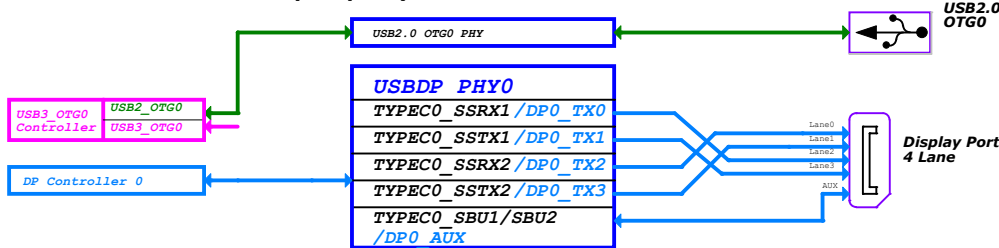
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



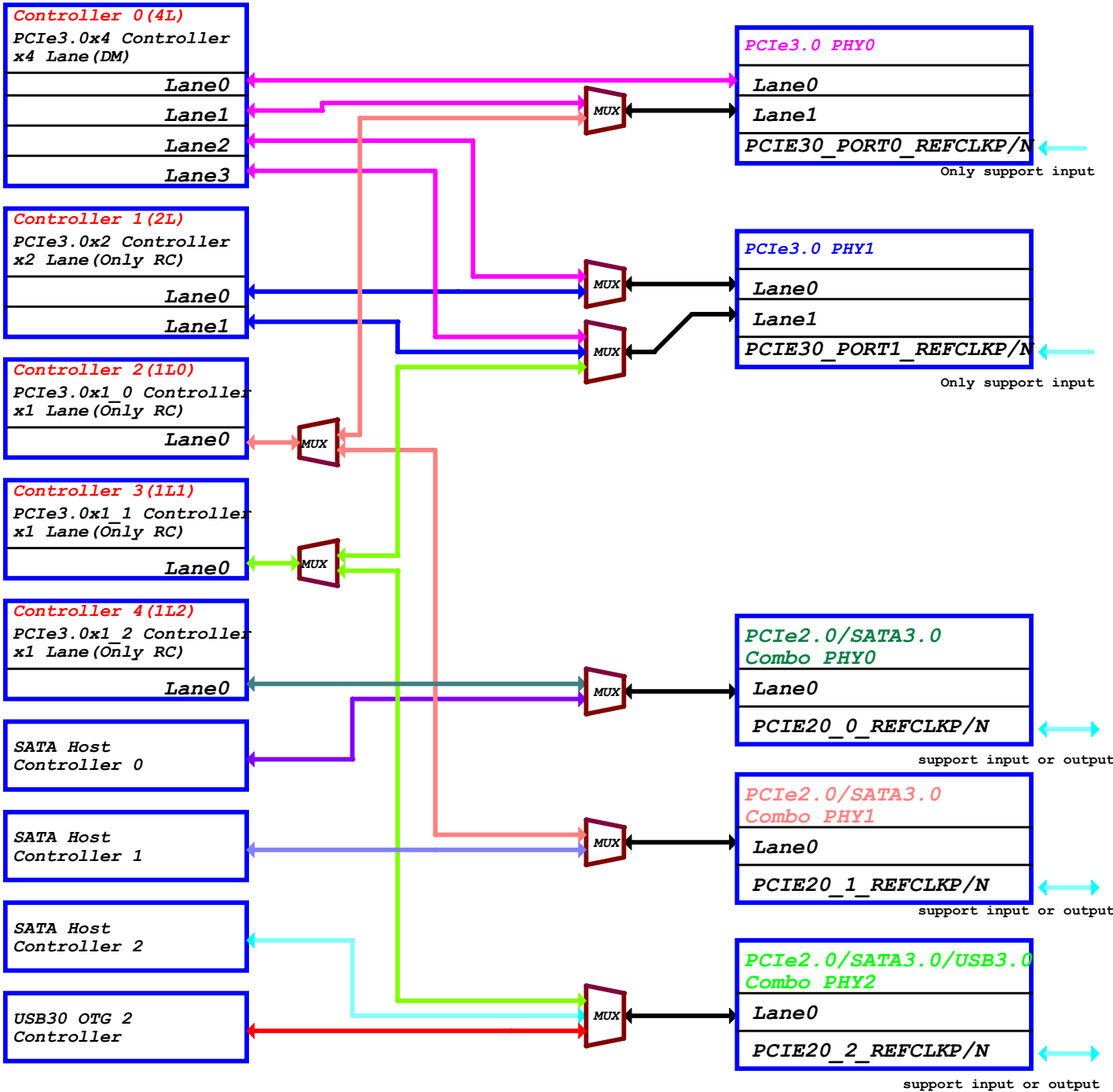
Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



PCIe/SATA Connector Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO & Power Pin
	OPTION	CLK LANE	DATA LANE	
PCIe30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIe30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIe30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
PCIe30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIe20X1_2 RC	OPTION1	PCIE20_0_REF_CLKP PCIE20_0_REF_CLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

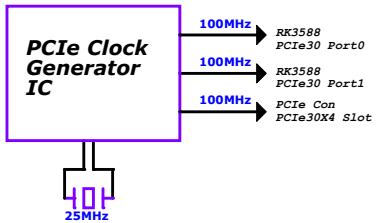
Note:
PCIE30_PORT*_REF_CLKP/N is input gpio
PCIE20_*_REFCLKP/N is output or input gpio

Note:
M*=Mean to M0 or M1, It's the same source, Just multiplex to M0 or M1. So, Only use one at the same time.

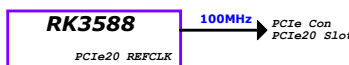
PCIe/SATA Function Combination

Function Combination				
Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



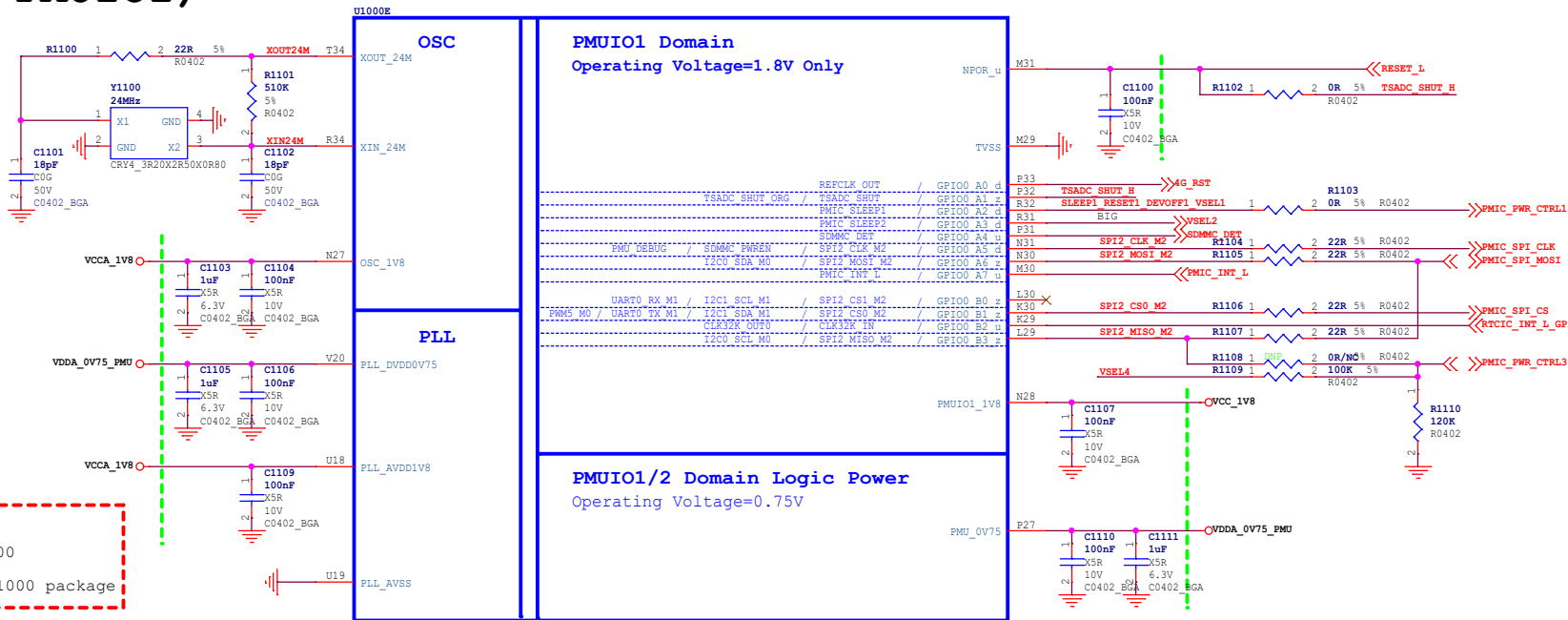
RK3588_E (OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification.

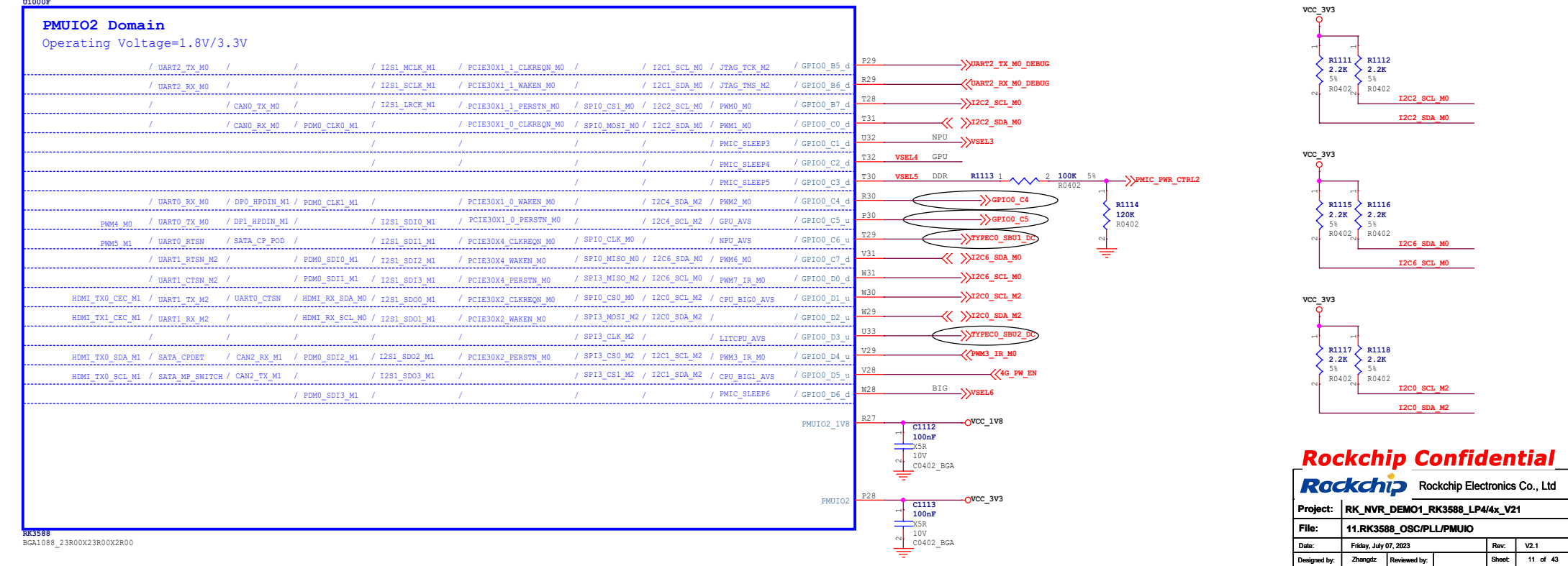
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$CL = (CL1 * CL2 / (CL1 + CL2)) + PCB\ strays$
Total CL<12pF

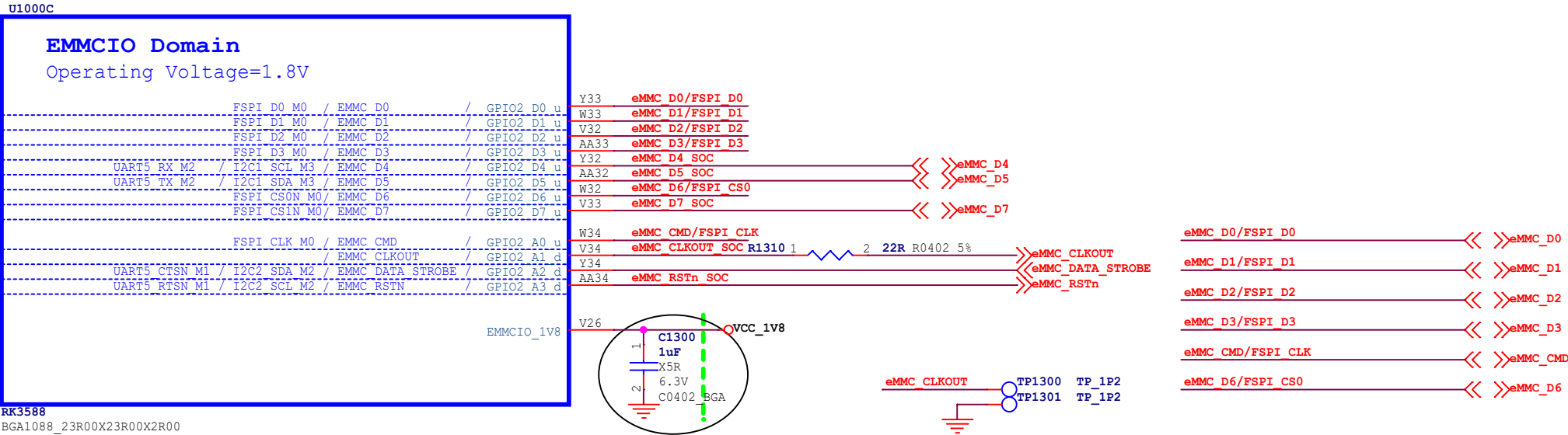
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



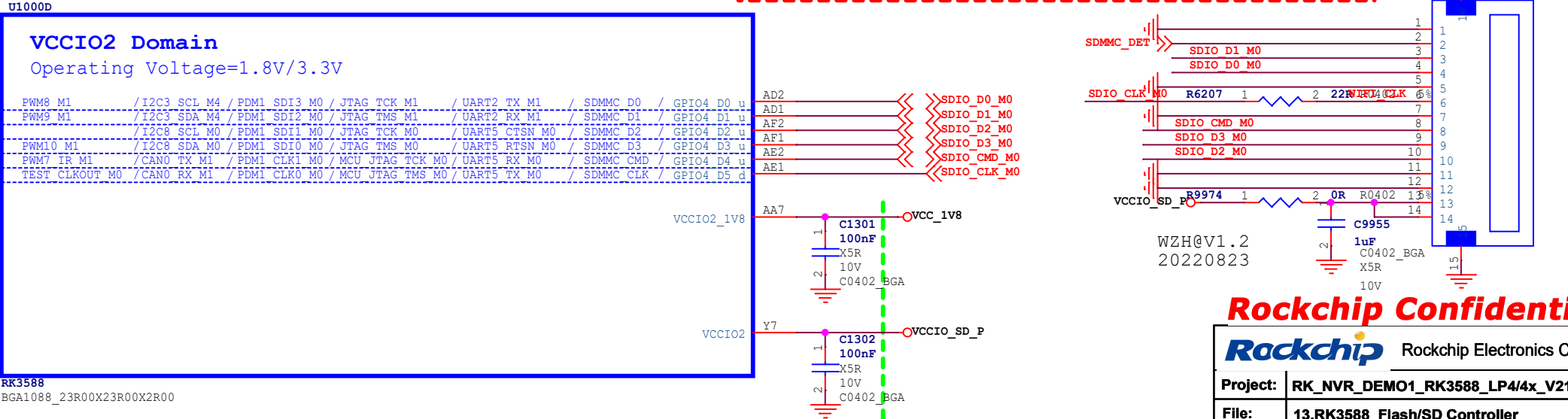
RK3588_F (PMUIO2)



RK3588_C (EMMCIO Domain)



RK3588_D (VCCIO2 Domain)



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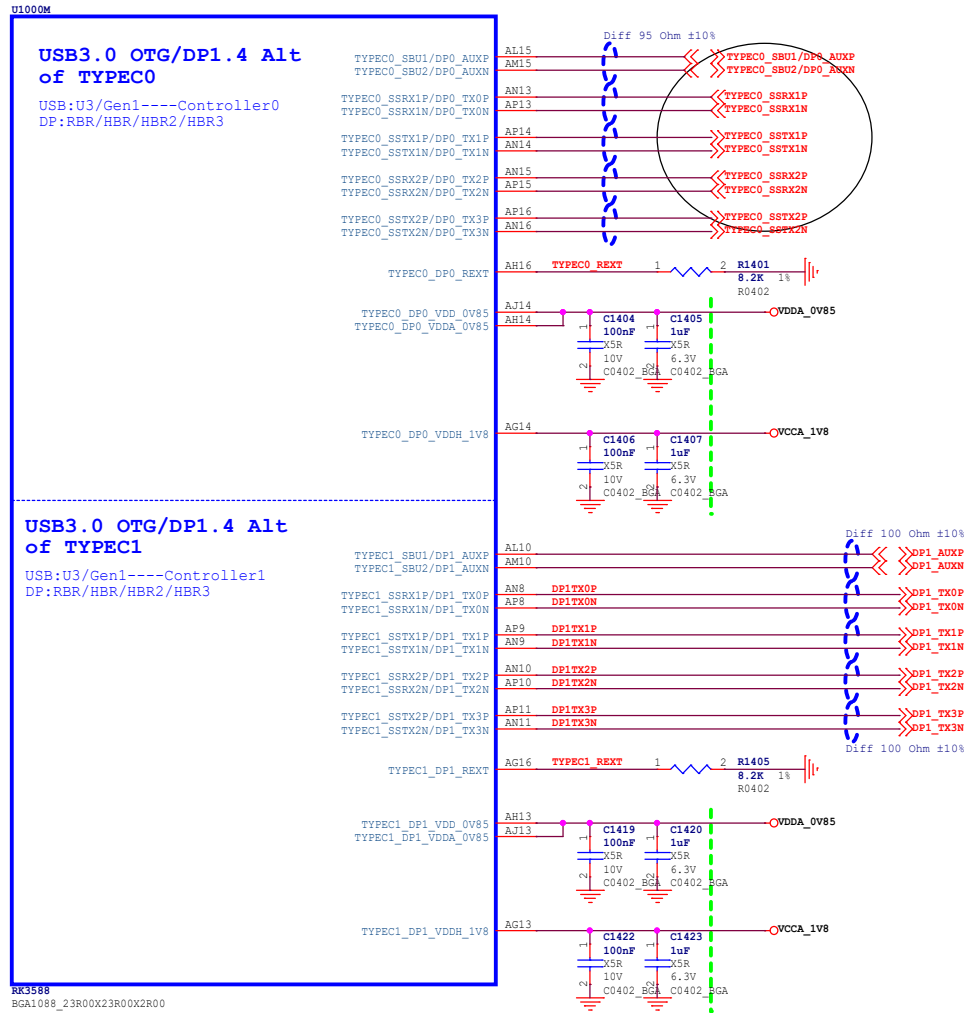
Rockchip Rockchip Electronics Co., Ltd

Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	13.RK3588_Flash/SD Controller		
Date:	Friday, July 07, 2023	Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	

Sheet: 13 of 43

RK3588_M(TYPEC/DP)

If TYPEC0 is not used,
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

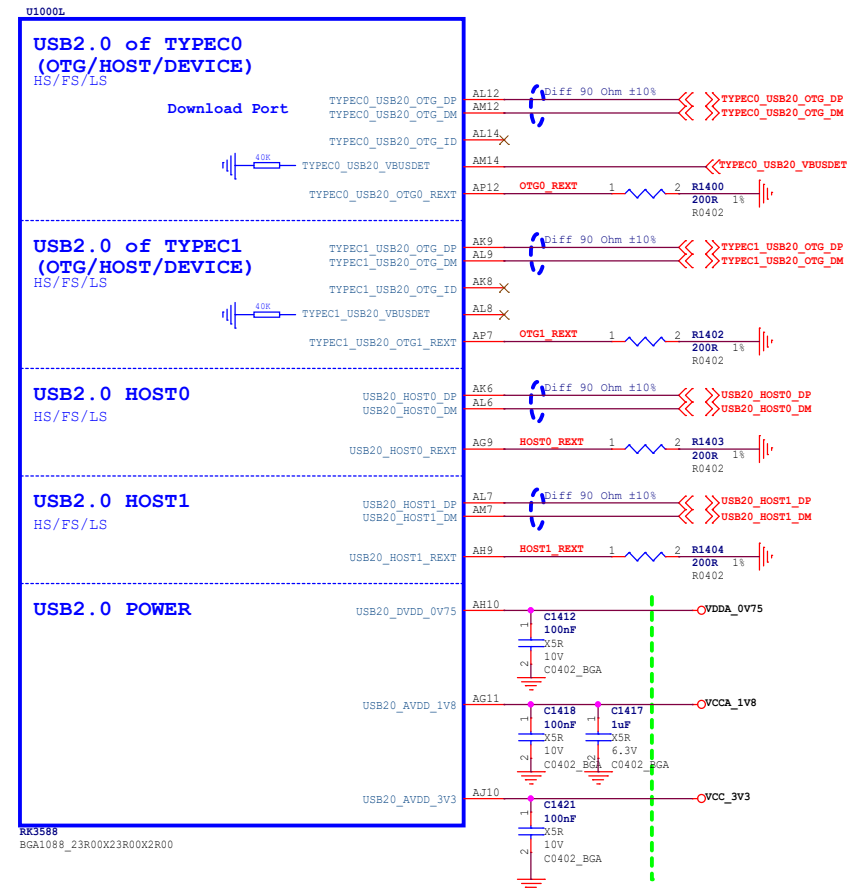


USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0~3
Option2	USB30 x4Lane	DP_TX_Lane0~3
Option3	USB30X2Lane+DPX2Lane	USB30: Lane0 Lane1 DP: Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30: Lane2 Lane3 DP: Lane0 Lane1

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588_L(USB2.0 HOST/OTG)



Note:

TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:

If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating

USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:

The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

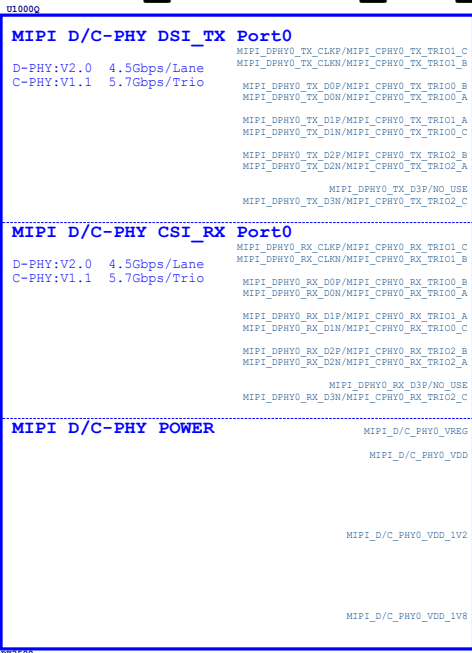
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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Rackchip Rockchip Electronics Co., Ltd

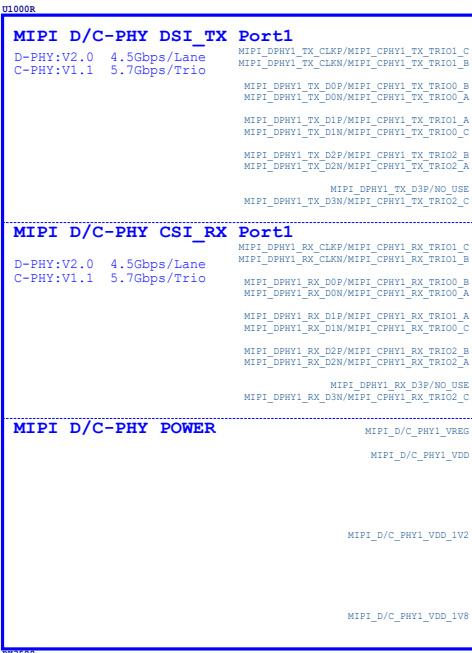
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	14.RK3588_USB30/USB20_Ctrl		
Date:	Friday, July 07, 2023	Rev:	V2.1
Designed by:	Zhangtz	Reviewed by:	
Sheet:	14	of 43	

RK3588_Q/R(MIPI_D/C_PHY0/1)



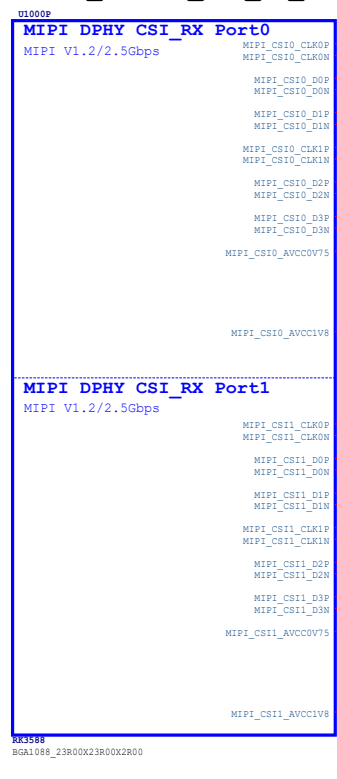
RK3588
BGA1088_23R00X23R00X2R00

If not used,
Signal: leave floating
Power: leave floating



RK3588
BGA1088_23R00X23R00X2R00

RK3588_P(MIPI_CSI_RX_PHY)



RK3588
BGA1088_23R00X23R00X2R00

If not used,
Signal: leave floating
Power: leave floating or tie to VSS

MIPI_CSI_RX Configuration

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:

When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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Rockchip Electronics Co., Ltd

Project:	RK_NVR_DEMO1_RK3588_LP4x4_V21		
File:	16.RK3588_MIPI Interface		
Date:	Friday, July 07, 2023	Rev:	V2.1
Designed by:	Zhangdt	Reviewed by:	Sheet 16 of 43

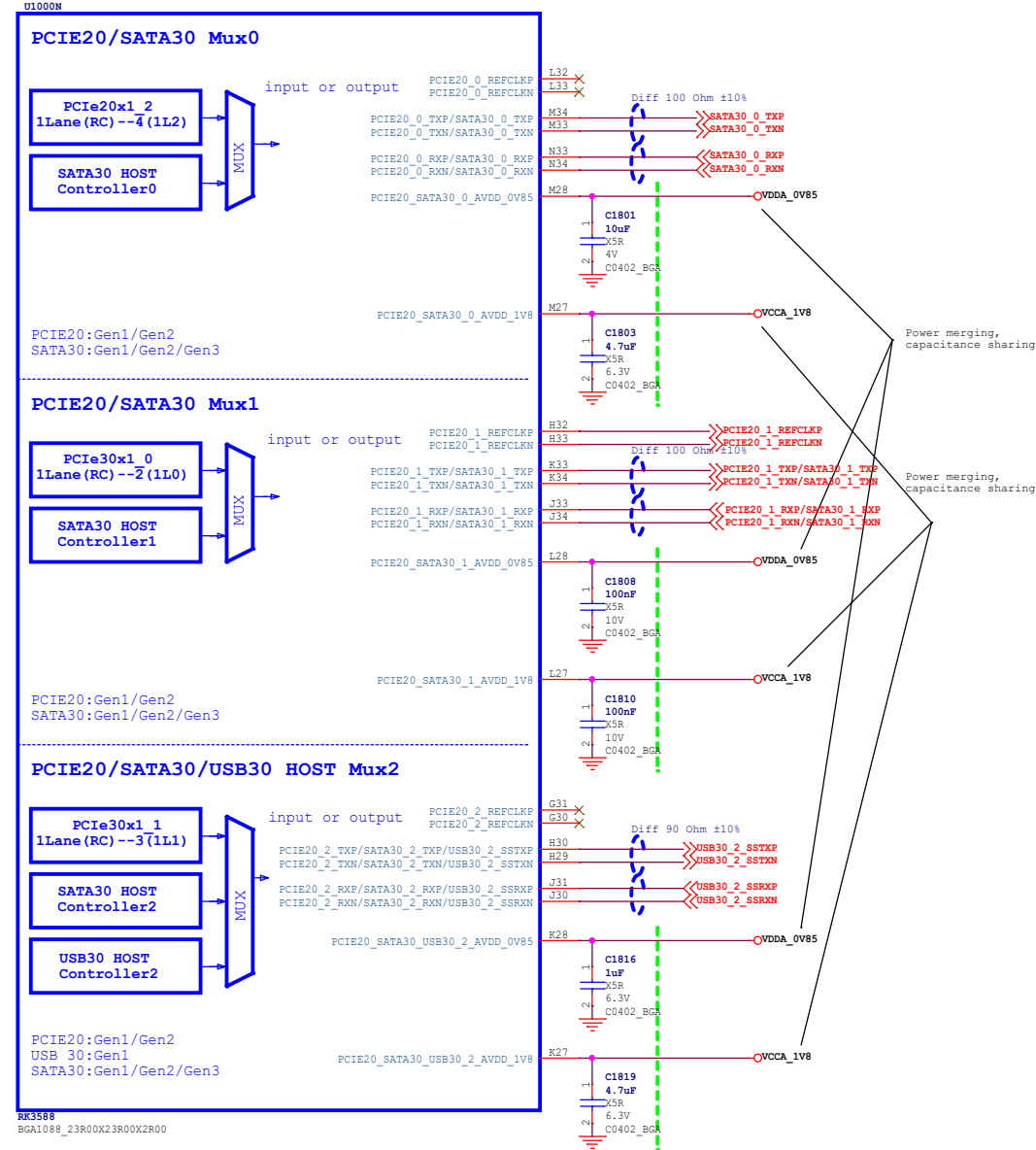
If not used,
Signal:leave floating
Power: Tie to VSS

```
If not used,
Signal:leave floating
Power: leave floating or tie to VSS
```

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3588_N (PCIE20)

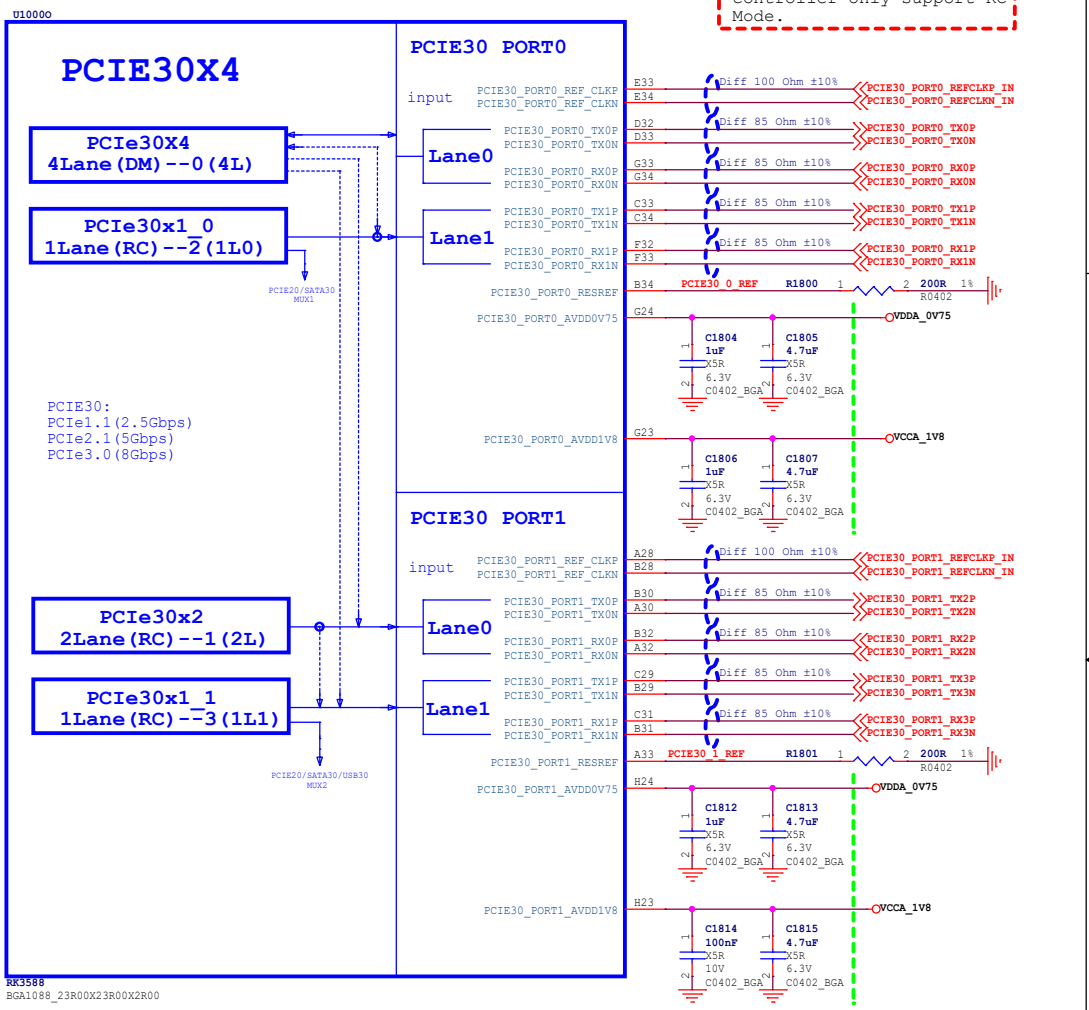
If not used,
Signal:leave floating
Power: Tie to VSS



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3588_O (PCIE30)

Note:
Only PCIE30 Controller 0
support RC and EP,Other
controller only support RC
Mode.



Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

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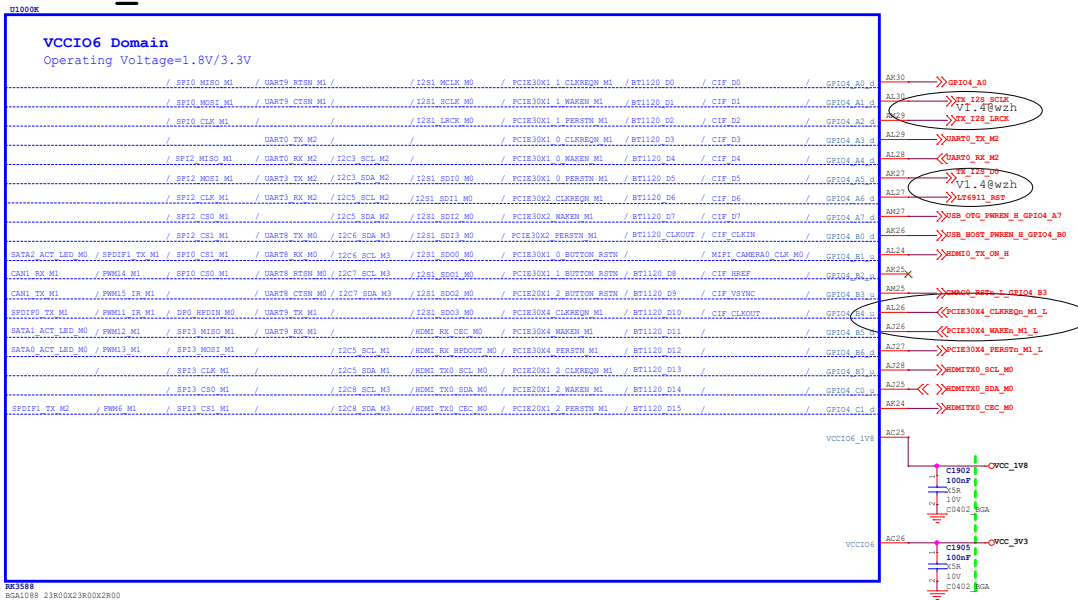
Rockchip Rockchip Electronics Co., Ltd

Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	18.RK3588_PCIE30/PCIE20/SATA30		
Date:	Friday, July 07, 2023	Rev:	V2.1
Designed by:	Zhangtz	Reviewed by:	
Sheet:	18 of 43		

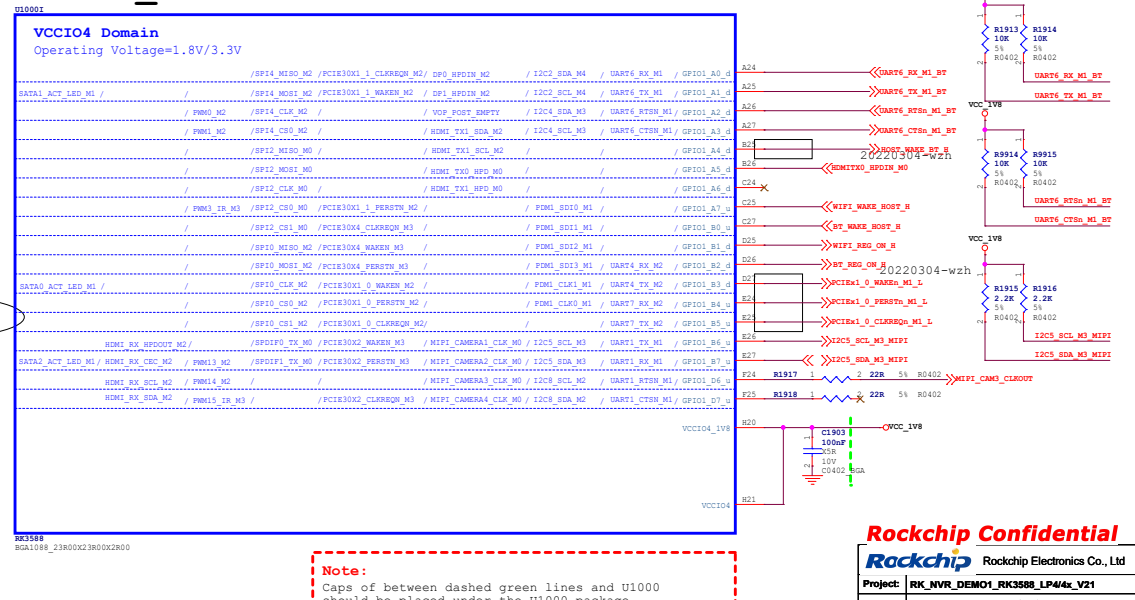
RK3588_J (VCCIO5 Domain)



RK3588_K (VCCIO6 Domain)



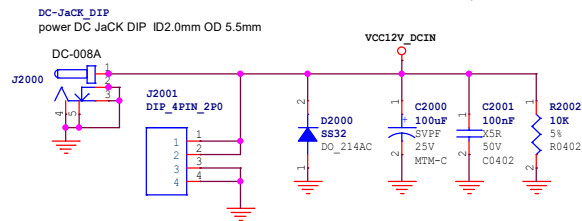
RK3588_I (VCCIO4 Domain)



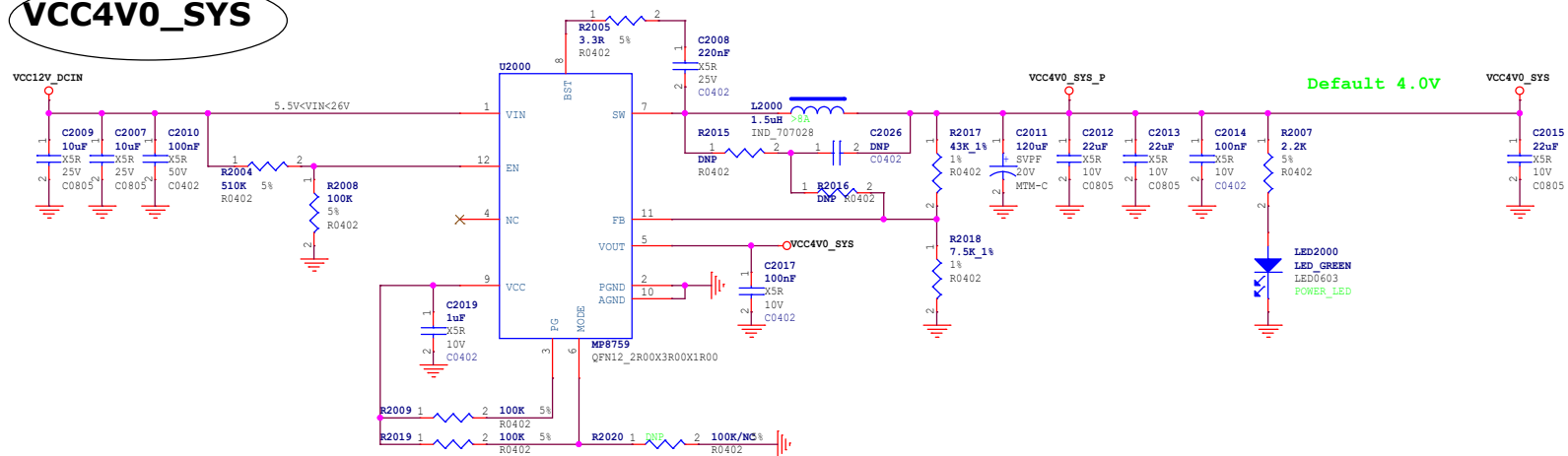
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

12V/3A DCIN

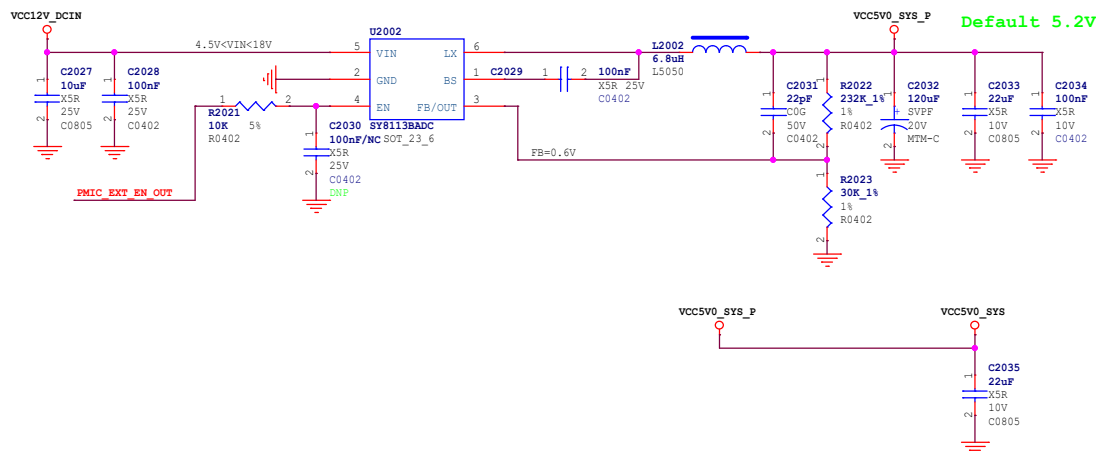
With SATA,PCIE, the current is estimated according to the actual number of SATA,PCIE



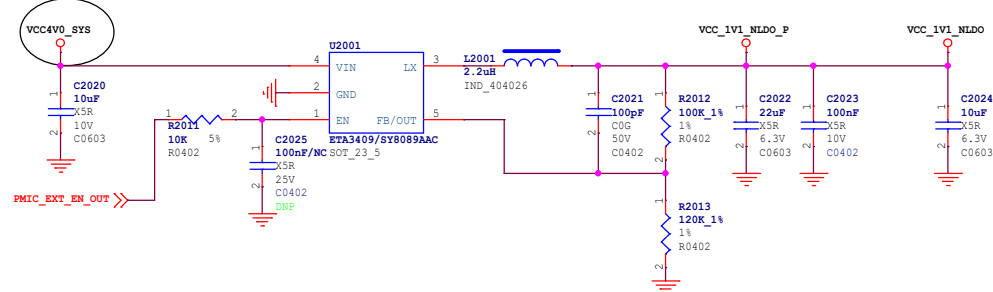
VCC4V0_SYS



VCC5V0_SYS



VCC_1V1_NLDO



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Rackchip Rockchip Electronics Co., Ltd

Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21

File: 20.Power_DC IN

Date: Friday, July 07, 2023

Designed by: Zhangtz

Reviewed by: Default

Rev: V2.1

Sheet: 20 of 43

 PMIC_SPI_CS
 PMIC_SPI_MOSI
 PMIC_SPI_CLK

 PMIC_PWR_CTRL1
 PMIC_PWR_CTRL2
 PMIC_PWR_CTRL3

 PMIC_INT_L

 RESET_L

 PMIC_EXT_EN_OUT



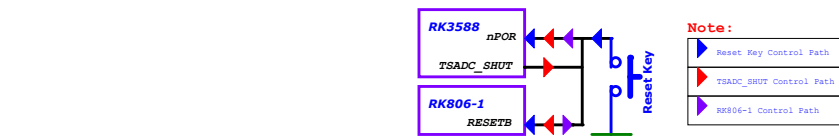
This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications

Operating Supply Voltage: 5.5V(5.25-6V)

Peak Pulse Current: >10A (tpw/20us)

Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

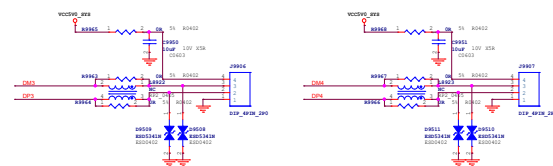
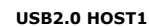
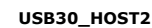
[illegible]

The diagram illustrates the PLDO power plane for the iZ22008. It shows the power distribution network, including input capacitors, decoupling capacitors, and various power pins. Key components include C2253, C2259, C2264, C2268, C2255, C2256, C2257, C2260, C2261, C2265, C2266, C2267, and C2269. The diagram also shows the connection to the iZ22008 chip and the output of the PLDO to the VDDA pins. The output voltage is 0.75V, and the current is 0.5A. The diagram includes a note: 'Default:0.85V;Low frequency:0.85V-->0.75V'.

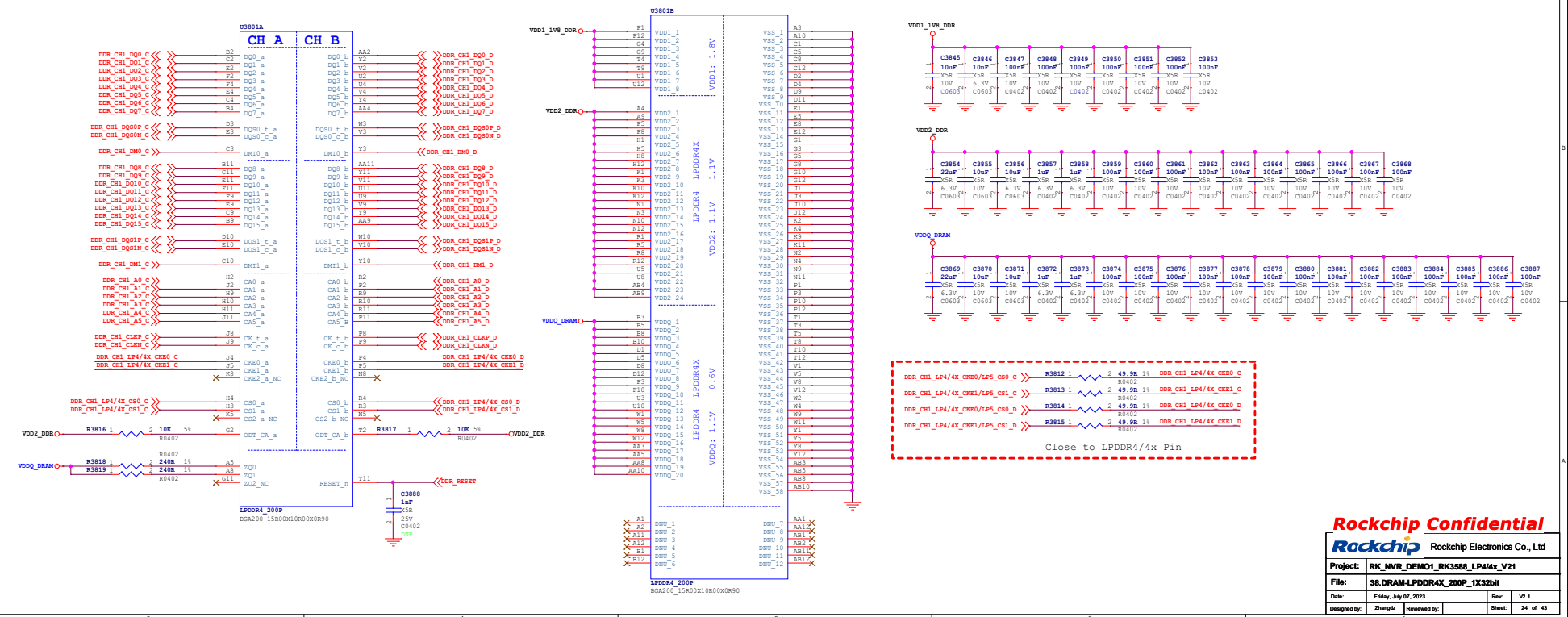
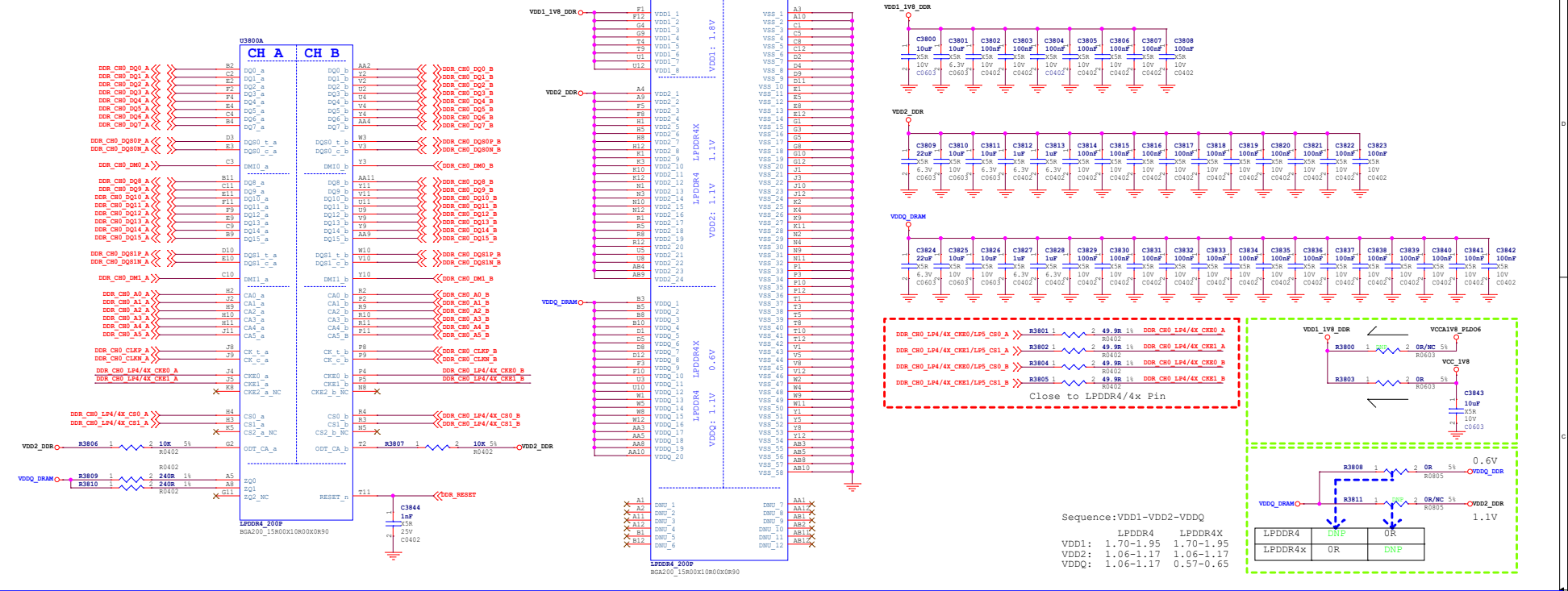
Note:
The RK806 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics,

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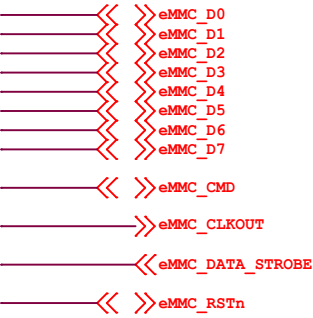
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21			
File:	22.Power-PMIC_RK806-1			
Date:	Friday, July 07, 2023		Rev:	V2.1
Designed by:	Zhouzhi	Reviewed by:	Debut	Sheet: 21 of 43



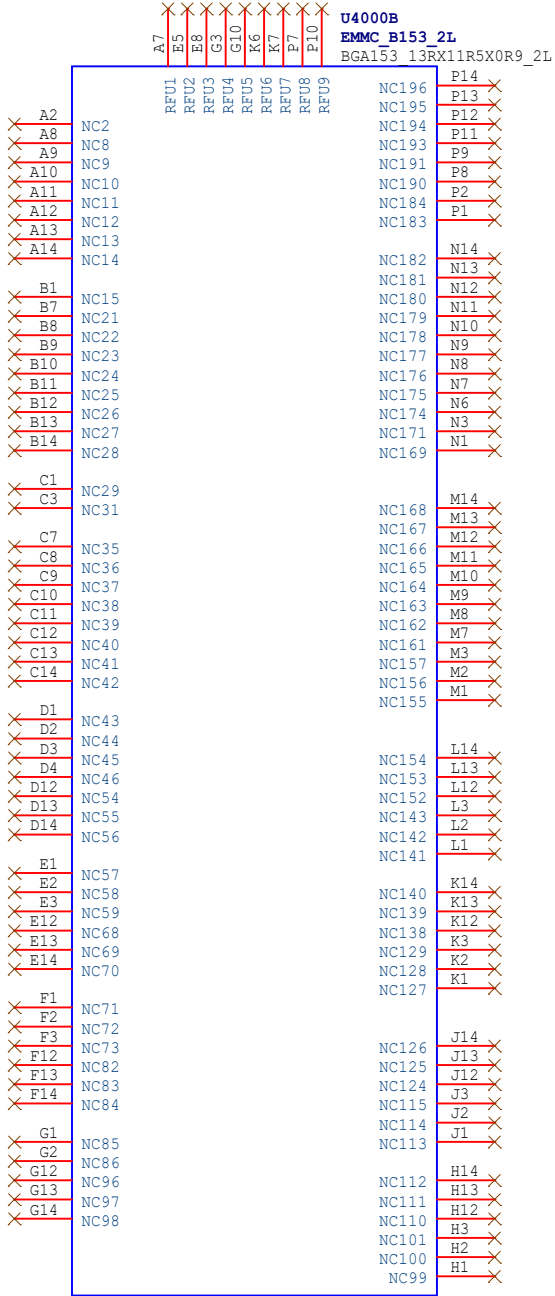
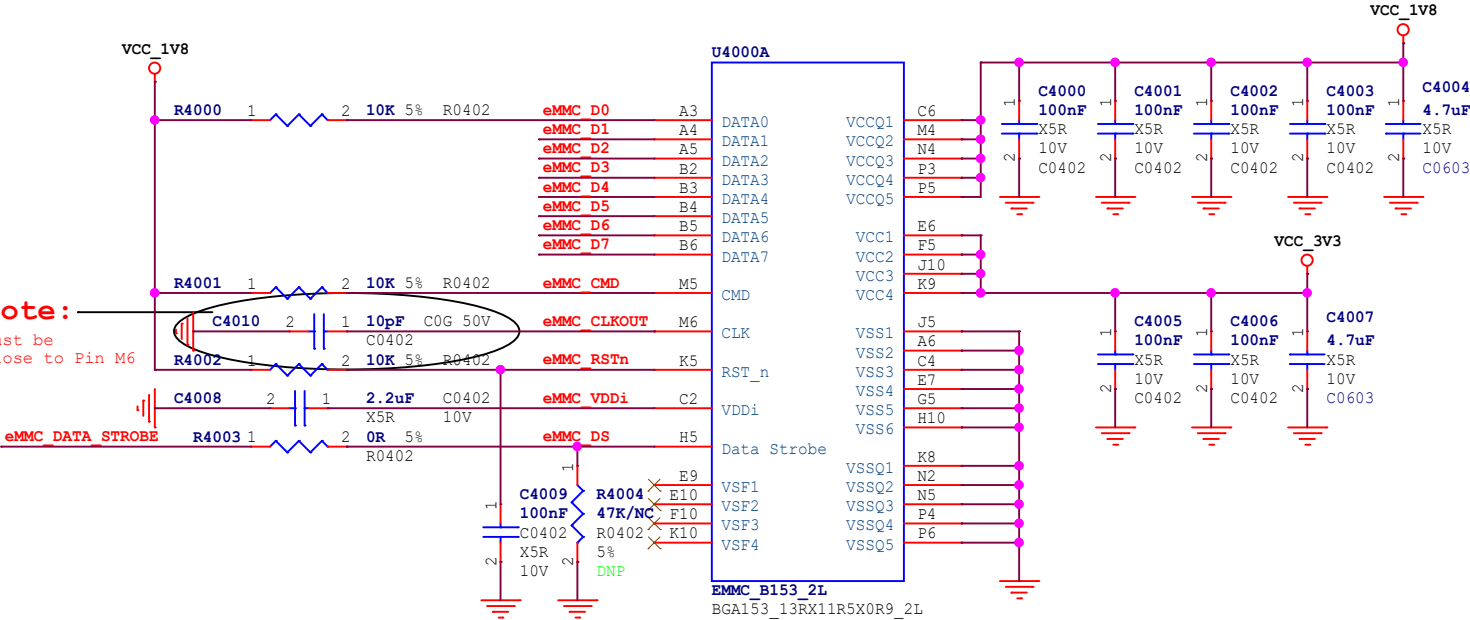
LPDDR4/4X



eMMC Flash



Note:
Must be close to Pin M6



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Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	40.Flash-eMMC Flash		
Date:	Friday, July 07, 2023	Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default
Sheet:	25 of 43		

SPI Flash

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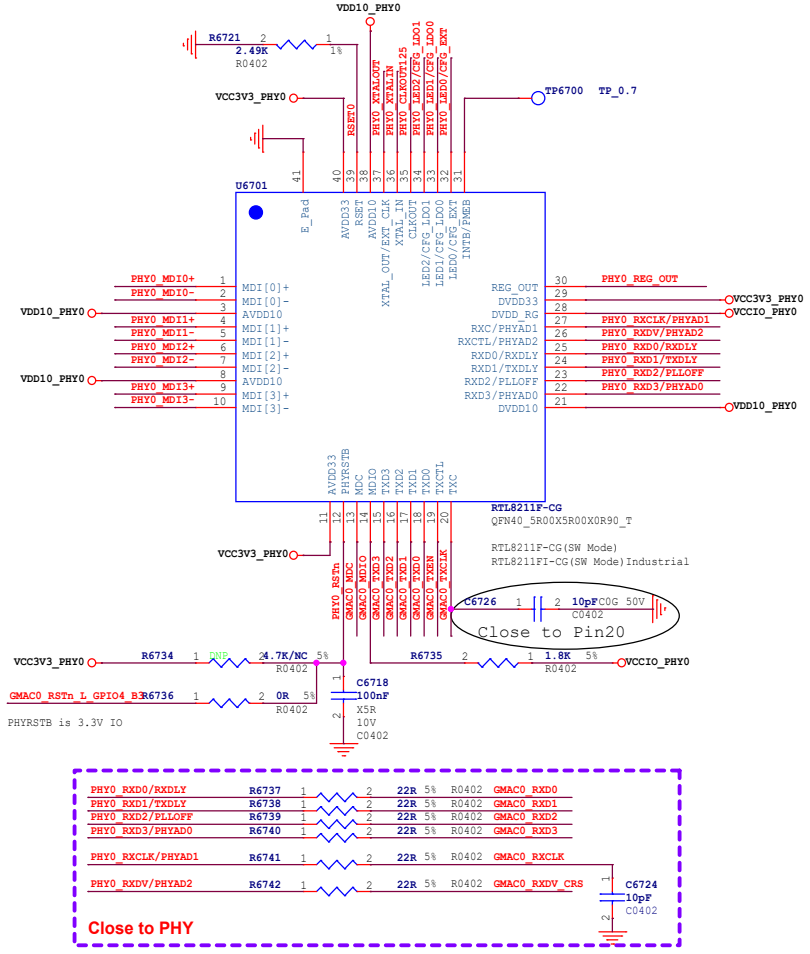
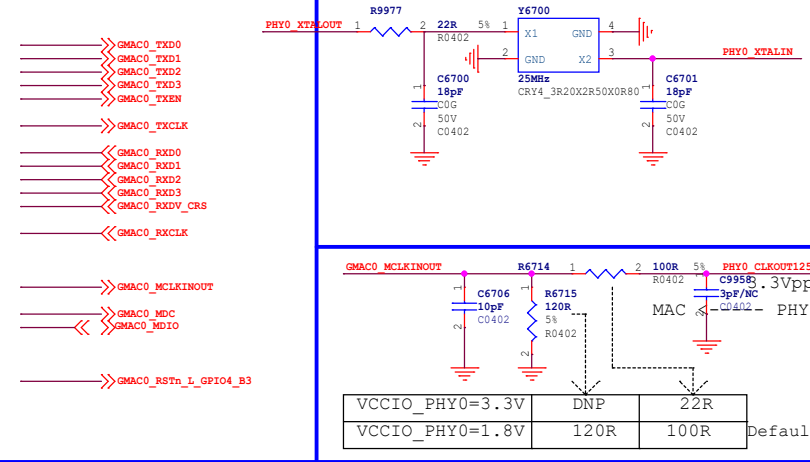
Rockchip Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	43.Flash-SPI FLASH(Optional)				
Date:	Friday, July 07, 2023			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	26 of 43

MIPI-CSIO_RX

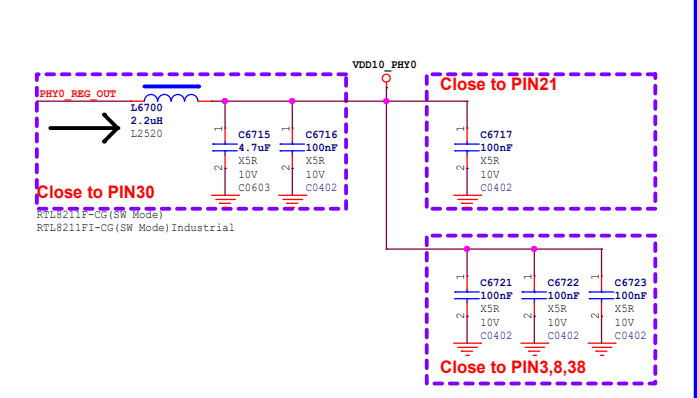
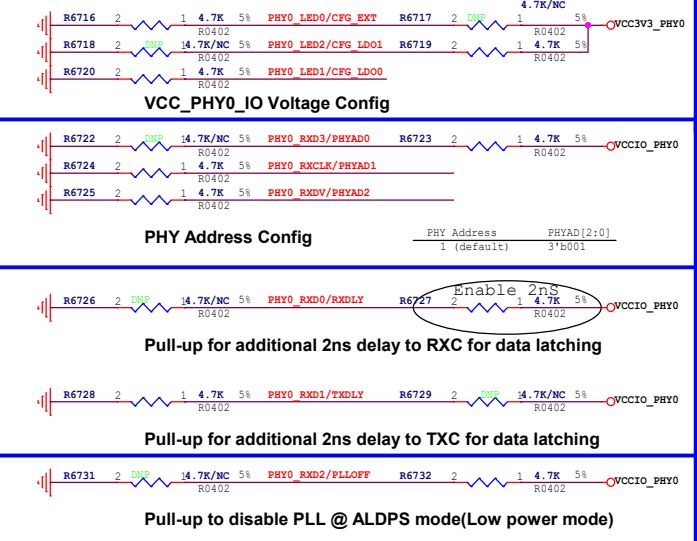
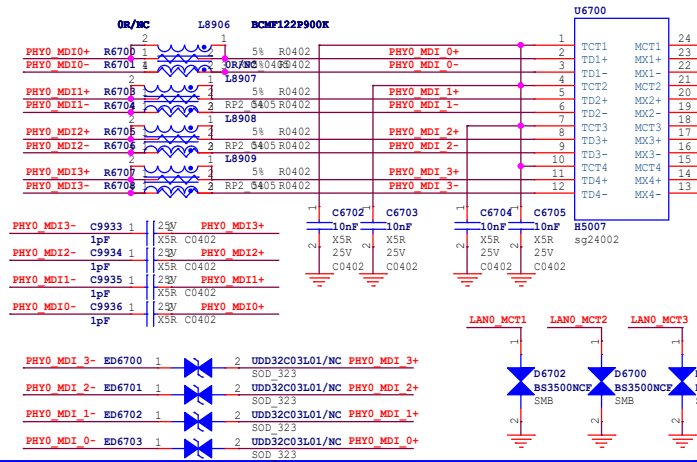


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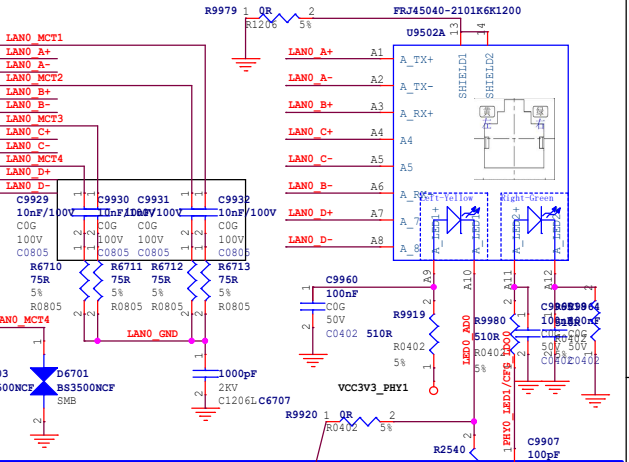
		Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	47.VI-Camera_MIPI-CSI				
Date:	Friday, July 07, 2023			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	27 of 43



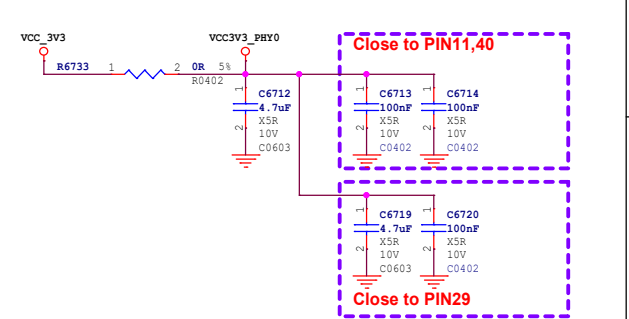
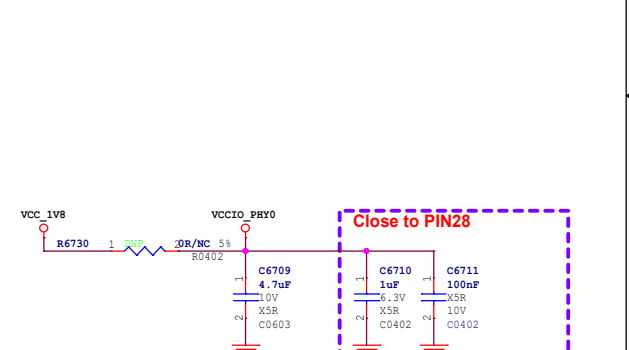
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RGMI Power Source	CFG EXT	CFG LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	



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Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21

File: 67.Ethernet-GEPHY_RGMII0

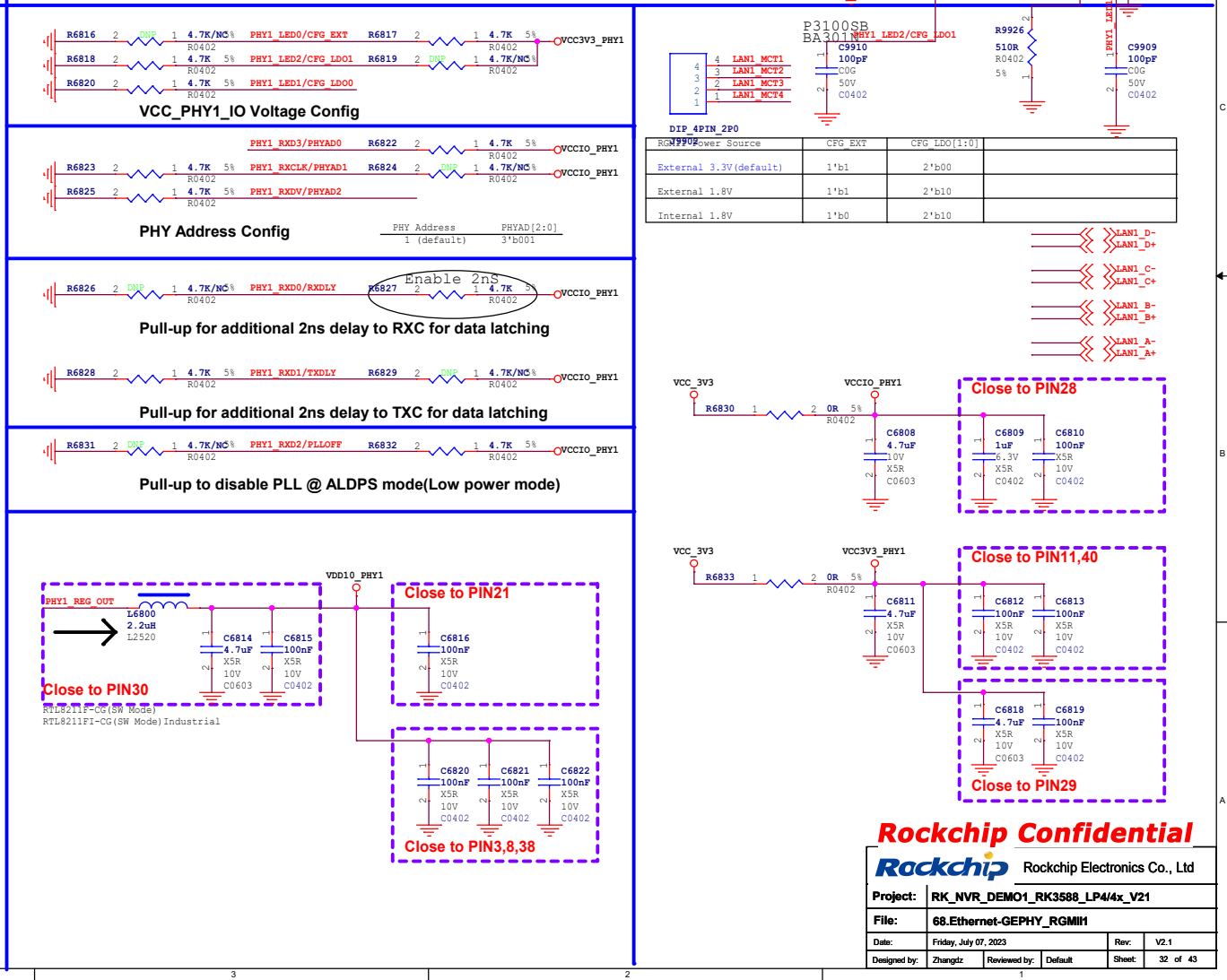
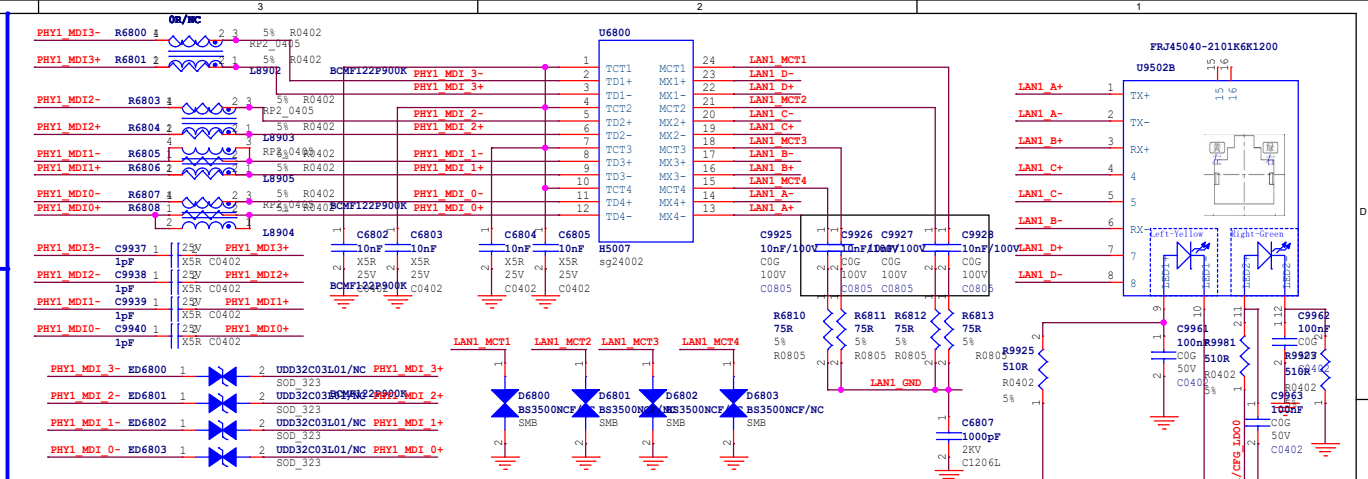
Date: Friday, July 07, 2023

Designed by: Zhangtz

Reviewed by: Default

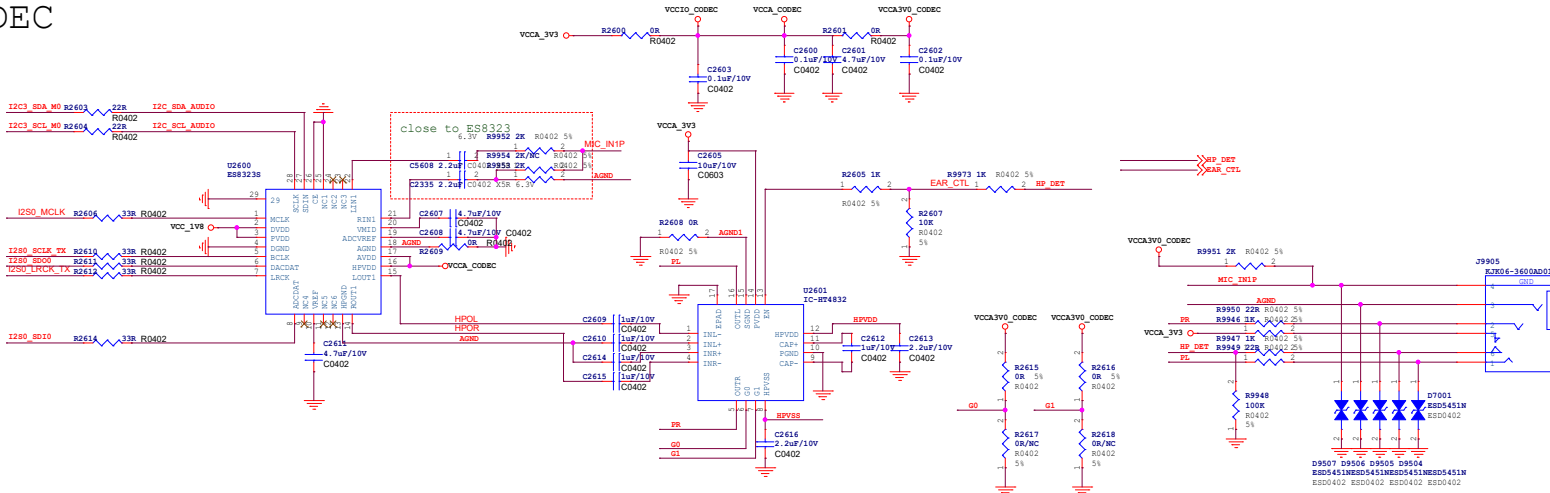
Rev: V2.1

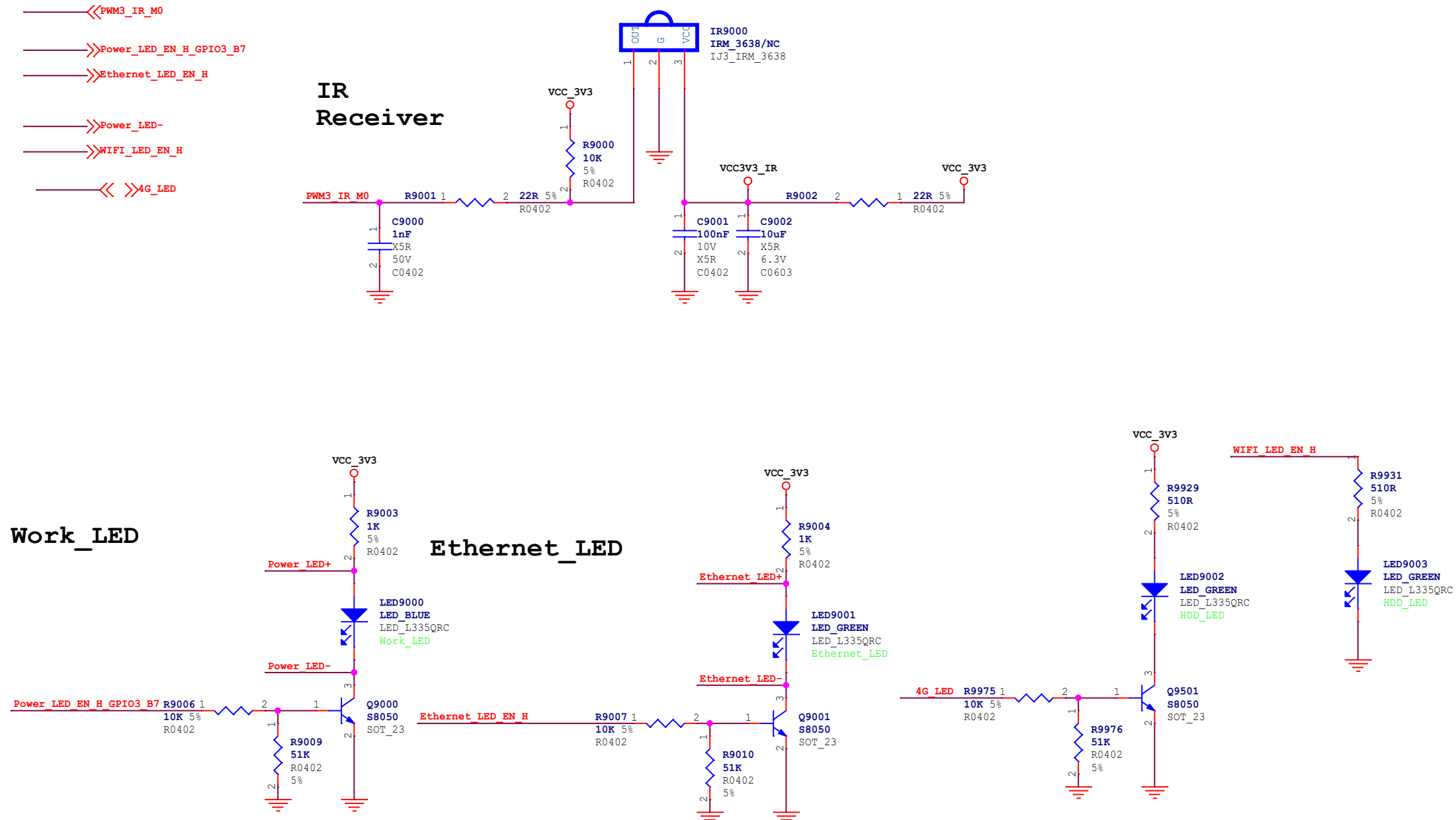
Sheet: 31 of 43



>>>I2S0_MCLK
>>>I2S0_SCLK_TX
>>>I2S0_LCLK_TX
>>>I2S0_BD00
<<<I2S0_BD10
<<<I2C3_BDA_MO
<<<I2C3_SCL_MO

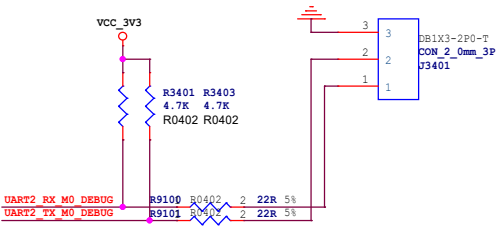
CODEC





Debug UART2

Option1



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Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21

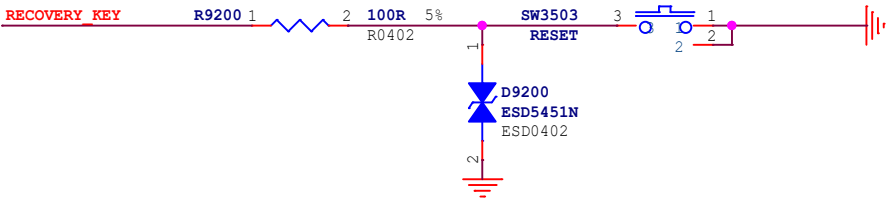
File: 91.Debug UART/JTAG

Date: Friday, July 07, 2023 **Rev:** V2.1

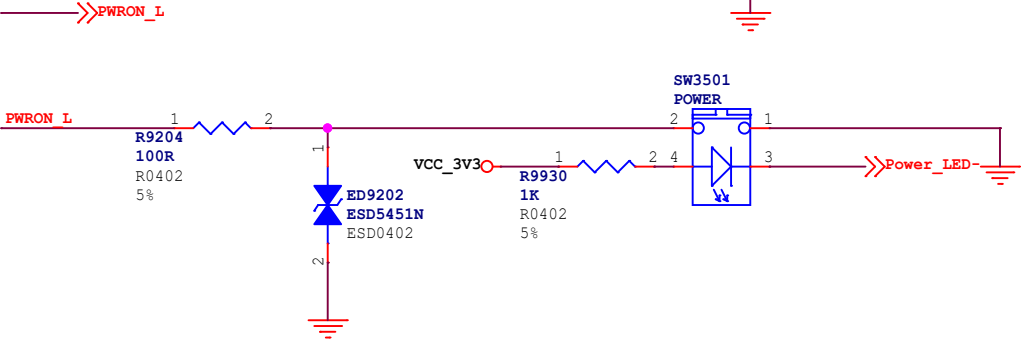
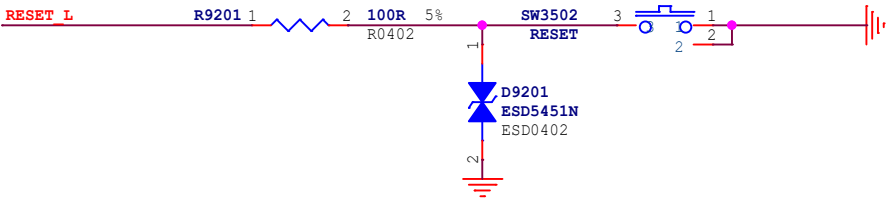
Designed by: Zhangtz **Reviewed by:** Default **Sheet:** 38 of 43

RECOVERY_Key

It is recommended to keep the circuit for the actual product update firmware



Reset_Key



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Rockchip Rockchip Electronics Co., Ltd

Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21

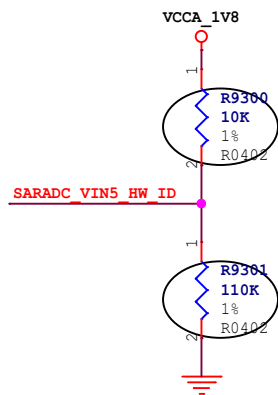
File: 92.KEY

Date: Friday, July 07, 2023 Rev: V2.1

Designed by: Zhangdz Reviewed by: Default Sheet: 39 of 43

<< SARADC_VIN5_HW_ID

HW_ID



SARADC_VIN1	Up Resistance	Down Resistance	AD value
HW_ID0	10K	DNP	4095
HW_ID1	10K	110K	3754
HW_ID2	20K	100K	3413
HW_ID3	33K	100K	3079
HW_ID4	18K	36K	2730
HW_ID5	36K	51K	2400
HW_ID6	51K	51K	2048
HW_ID7	51K	36K	1695
HW_ID8	36K	18K	1365
HW_ID9	100K	33K	1016
HW_ID10	100K	20K	683
HW_ID11	110K	10K	341
HW_ID12	DNP	10K	0

V10

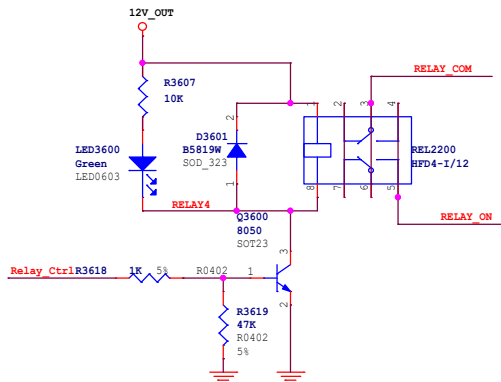
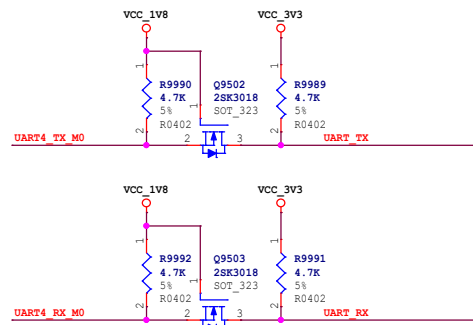
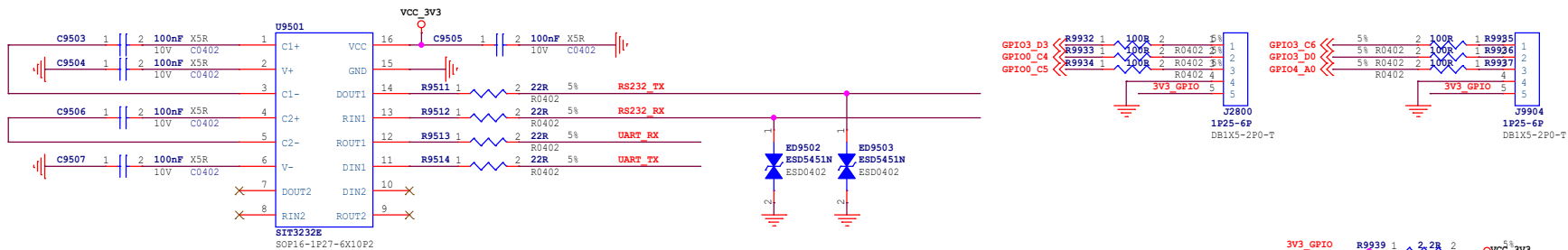
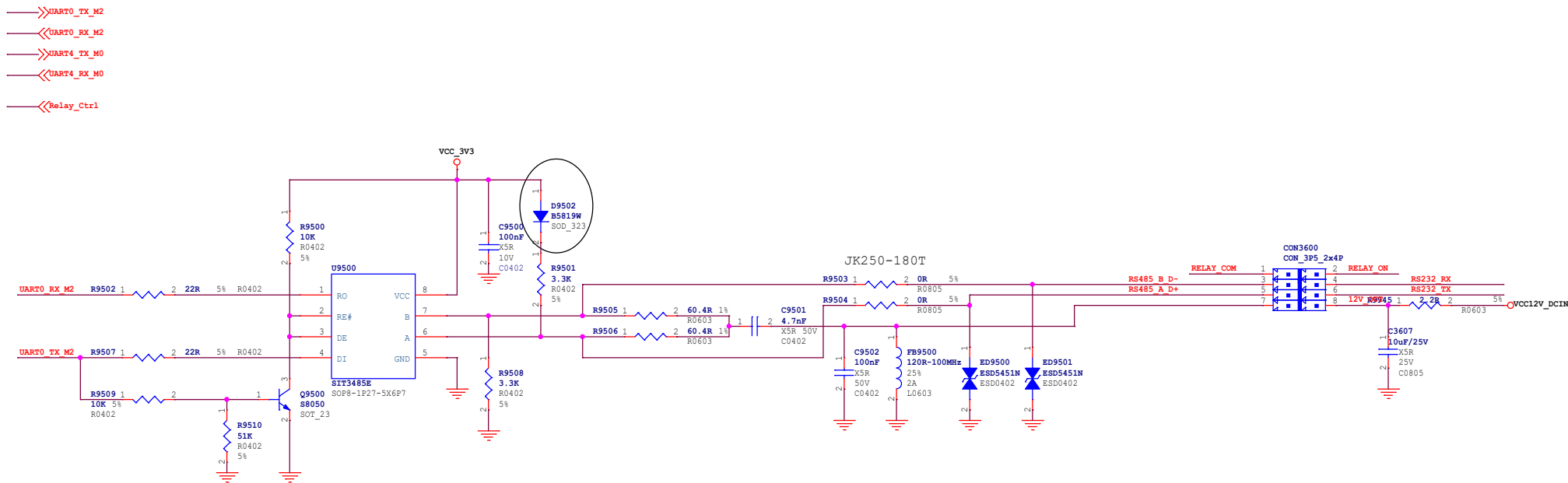
V21

Rockchip Confidential

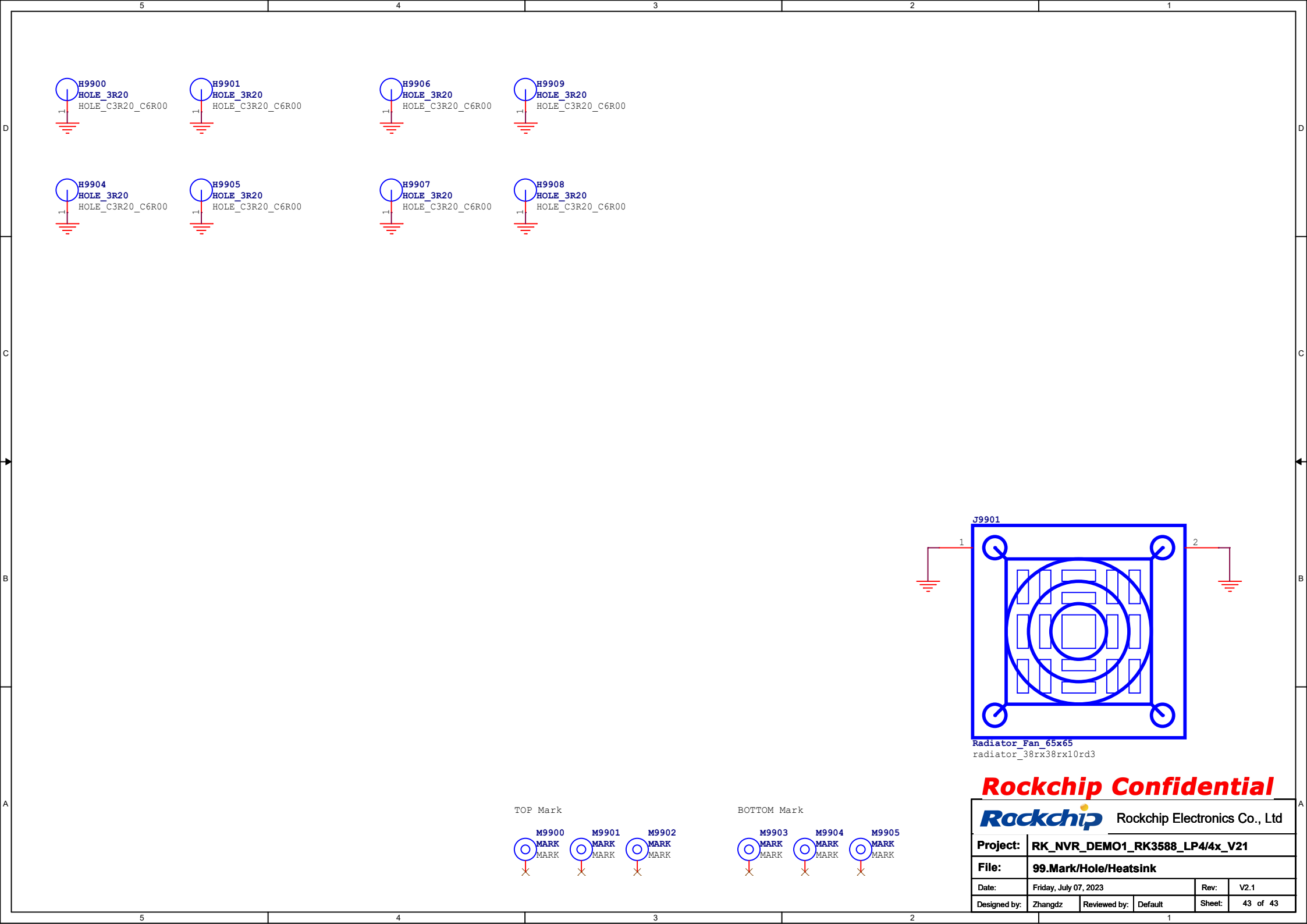


Rockchip Electronics Co., Ltd

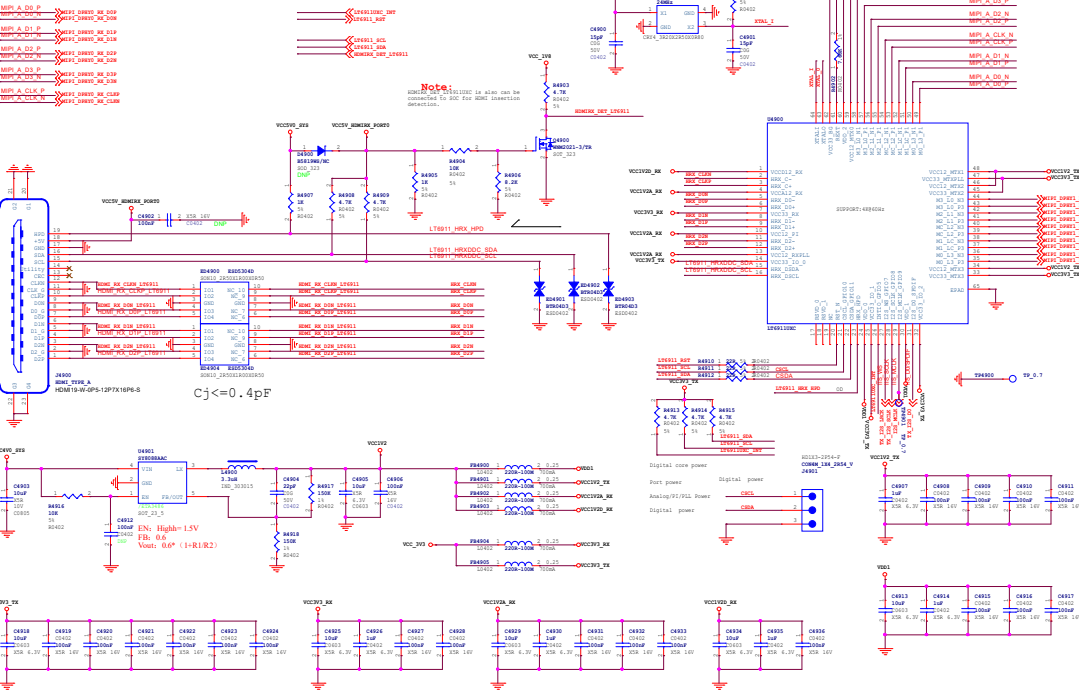
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	93.HW_ID		
Date:	Friday, July 07, 2023		Rev: V2.1
Designed by:	Zhangdz	Reviewed by:	Default
Sheet:		40 of 43	



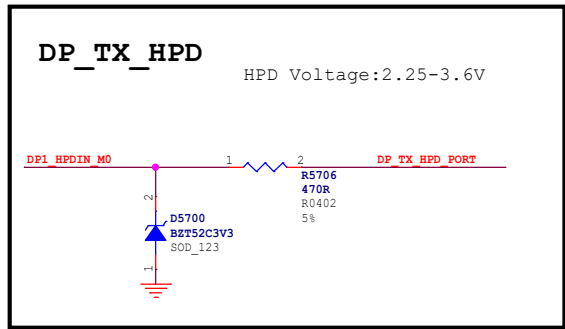
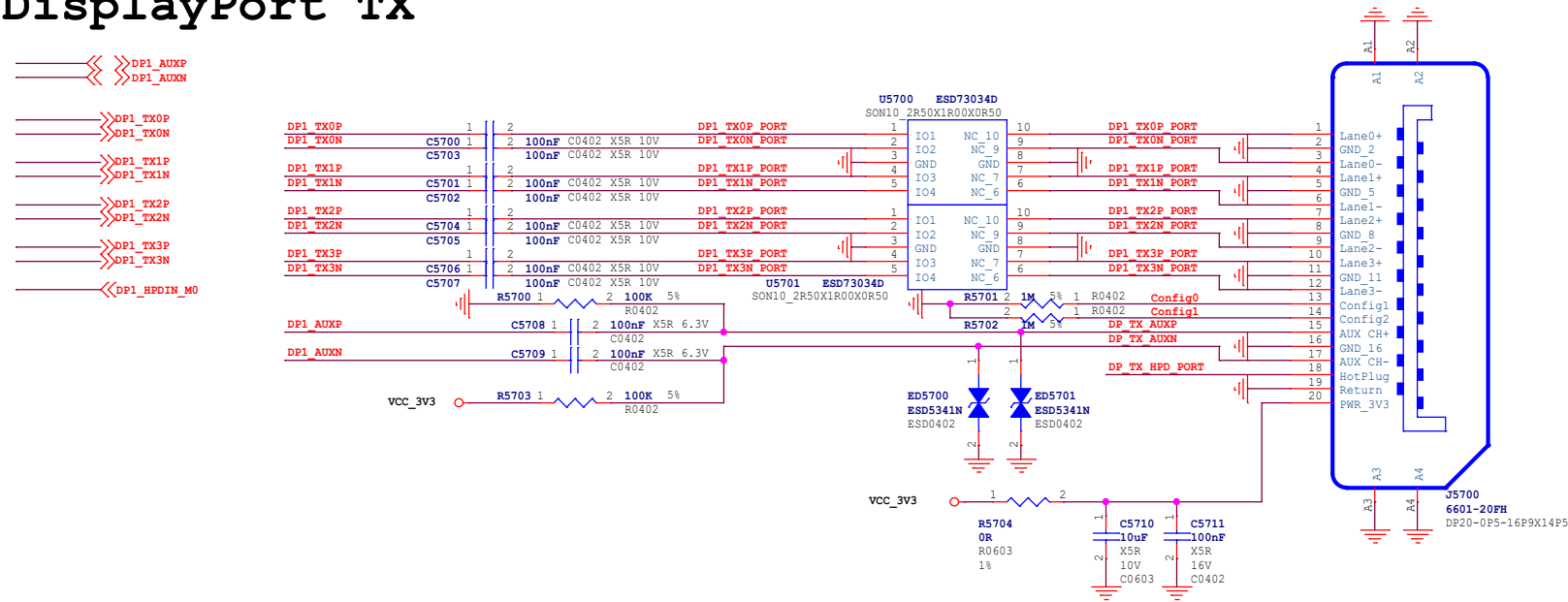
Pin1:DCD,<---,Data Carrier Detect
Pin2:RXD,<---,Receive Data
Pin3:TXD,<---,Transmit Data
Pin4:DTR,<---,Data Terminal Ready
Pin5:COM
Pin6:DSR,<---,Data Set Ready
Pin7:RTS,<---,Request to Send
Pin8:CTS,<---,Clear to Send
Pin9:RI ,<---,Ring Indicator



HDMI2.0 RX(OPTION2)



DisplayPort TX



ShenZhen HugSun Technology Co., Ltd

Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21

File: 51.DP

Date: Friday, July 07, 2023

Designed by: Wang

Rev: V1.0

Sheet: 51 of 99

