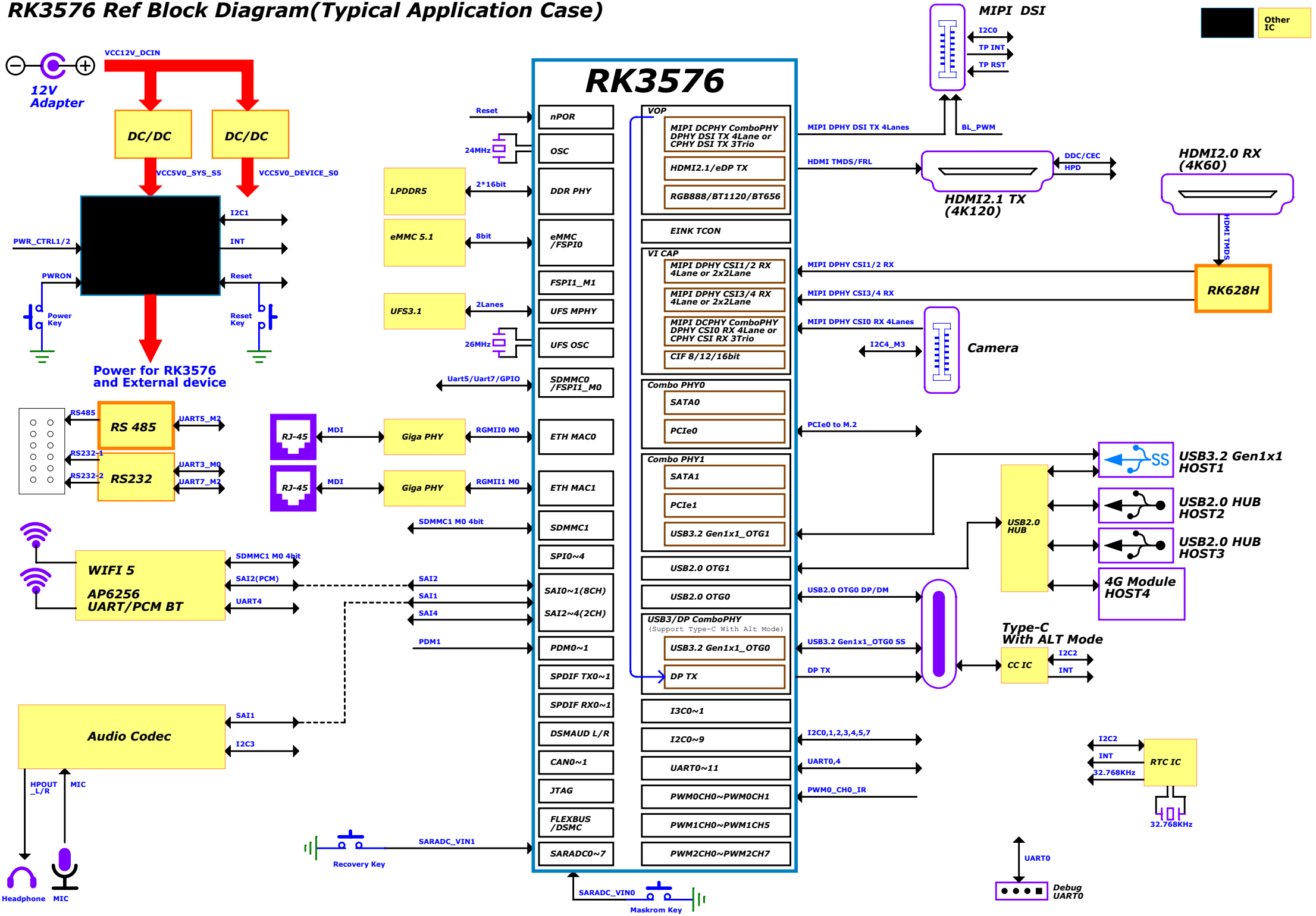
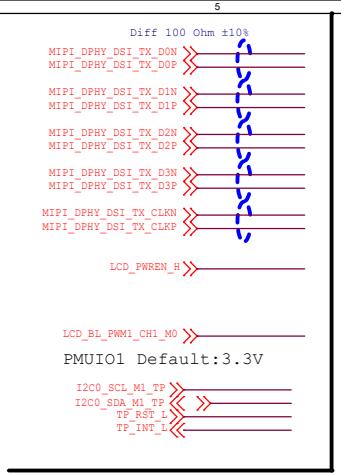
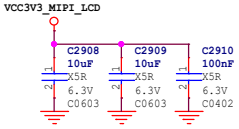
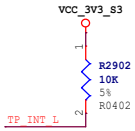
RK3576 Ref Block Diagram(Typical Application Case)

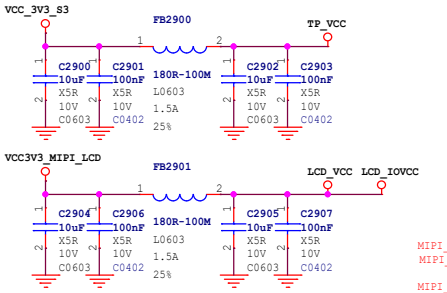


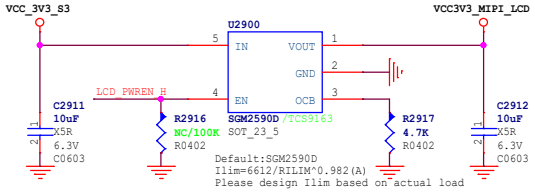
MIPI LCM

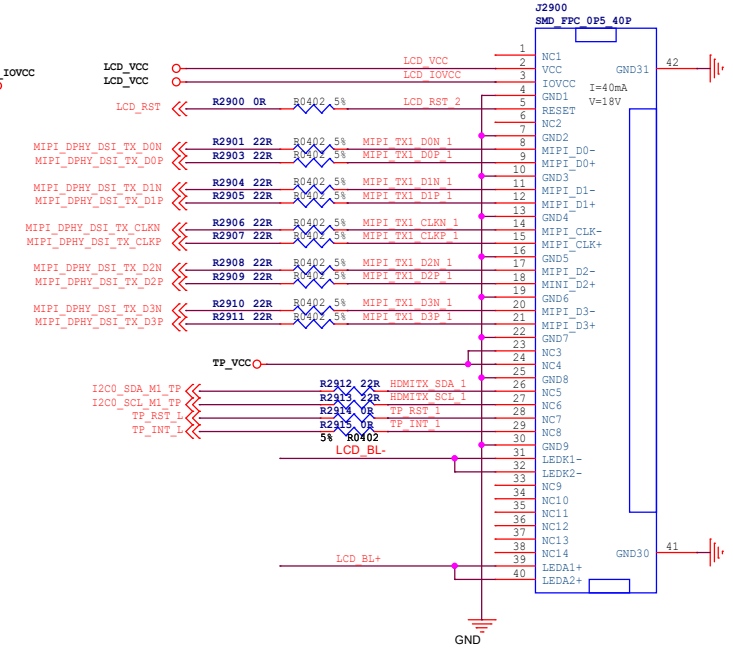




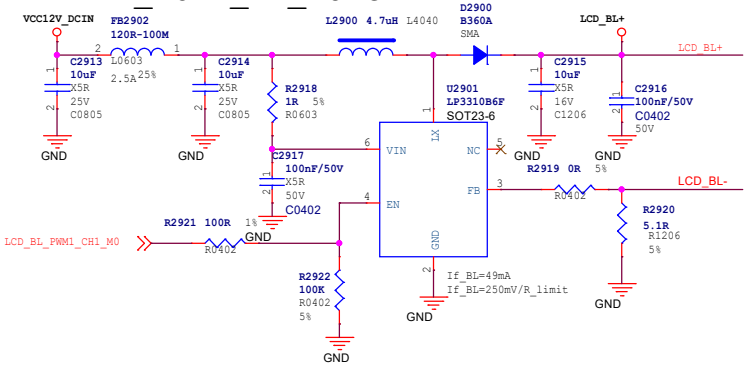








MIPI_LCD1_BL_Power



REF Schematic for RK3576

Main Functions Introduction

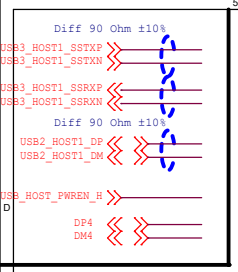
1) PMIC: 1 x RK806S-5 + DiscretePower
2) RAM: 1 x LPDDR4X 32bit
   Option: 1 x LPDDR4 32bit
   Option: 1 x LPDDR5 32bit
3) ROM: 1 x eMMC5.1 + 1 x UFS
   Option: 1 x SPI Flash(FSPI0)
4) Support: 1 x Micro SD Card3.0
   Option: 1 x SPI Flash(FSPI1)
5) Support: 1 x USB TYPEC with Displayport Alt Mode
   Option: 1 x USB2.0
   Option: 1 x USB3.2 Gen1x1 HOST
6) Support: 3 x USB2.0 HOST(USB2.0 HUB) + 1 x USB3.2 Gen1x1 HOST(USB2.0 from HUB)
7) Support: 1 x a/b/g/n/ac/ax 2T2R SDIO WIFI6 + UART/PCM BT
   Option: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
   Option: 1 x a/b/g/n/ac/ax 2T2R SDIO WIFI + UART/PCM BT
   Option: 1 x a/b/g/n/ac 1T1R SDIO WIFI + UART/PCM BT
8) Support: 1 x PCIe Slot_36P
   Option: 1 x a/b/g/n/ac/ax 2T2R PCIe WIFI6 + UART/PCM BT
   Option: 1 x MiniPCIe Slot_with 4G
   Option: 1 x SATA Slot
9) Support: 3 x CAM MIPI CSI RX
   Option: 1 x 4Lanes MIPI DPHY RX Camera + 1 x HDMI RX to MIPI CSI
10) Support: 1 x LCM MIPI DSI TX
11) Support: 1 x HDMI2.1 TX (Up to 4Kx2K@120Hz)
   Option: 1 x LCM eDP TX
12) Support: 2 x 10/100/1000M Ethernet
   Option: 1 x 10/100M Ethernet + 1 x 10/100/1000M Ethernet
13) Support: 1 x Headphone + 2 x SPK + 1 x Analog MIC
   Option: 4 x PDM-DMIC
14) Support: 1 x SPDIF TX + 1 x SPDIF RX
15) Support: 1 x IR Receiver
16) Support: 1 x G-Sensor
17) Support: Array Key(MENU,VOL+,VOL-,ESC)
18) Support: 7 x SARADC + 1 x SARADC only for boot
19) Support: 1 x Debug UART Connector

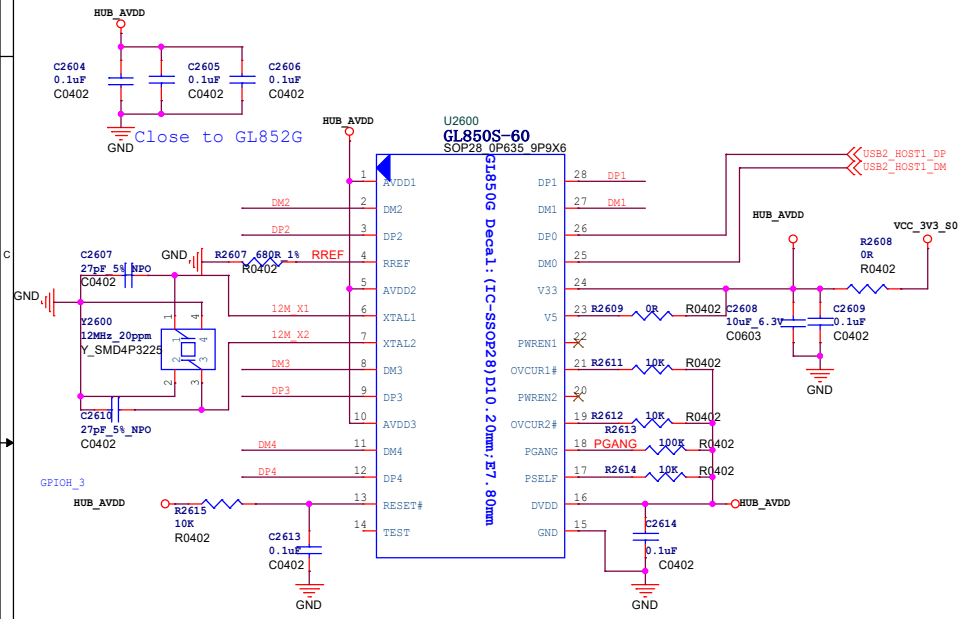
Note:

The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic.
If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	00.Cover Page				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	1 of 63

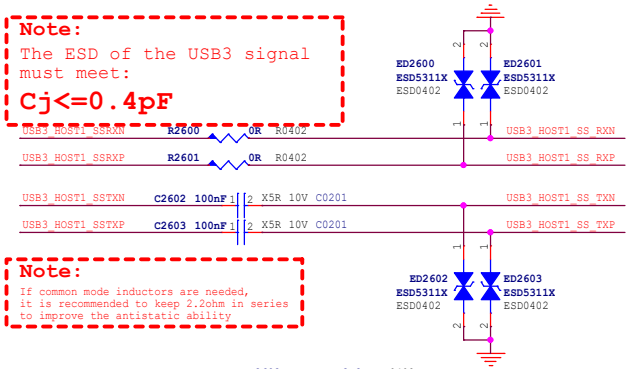
MODE1(Default):
USB20_HUB+USB3.0 HOST

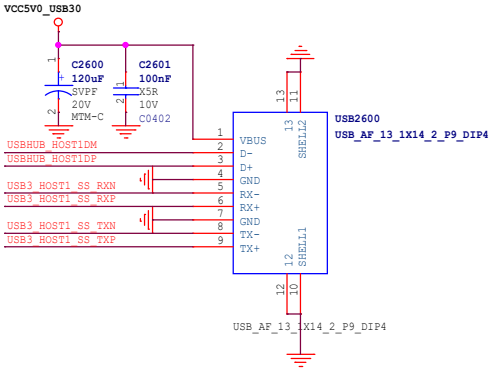


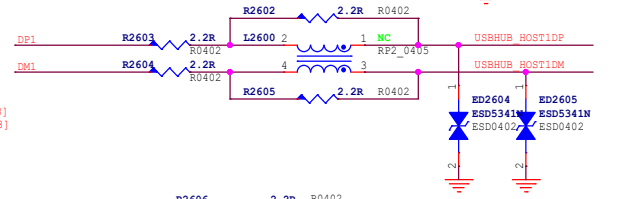


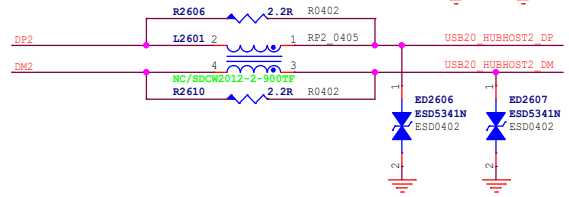
Note:
The ESD of the USB3 signal must meet:
Cj<=0.4pF

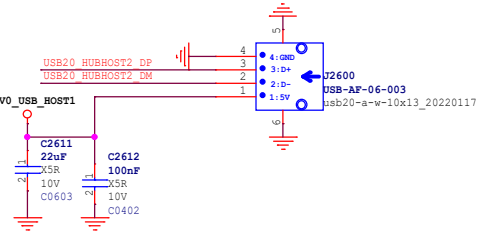
Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability



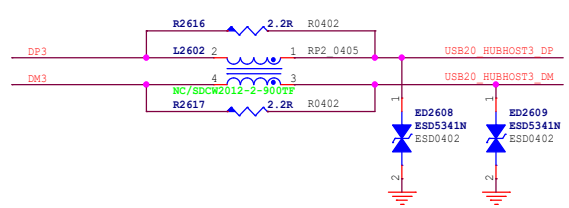


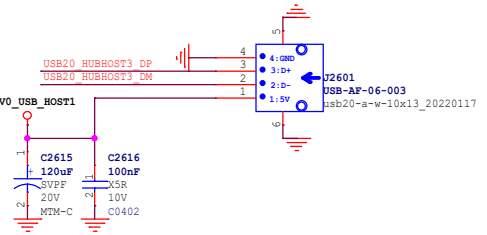




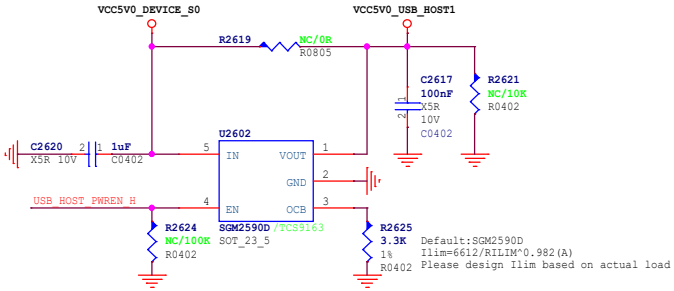


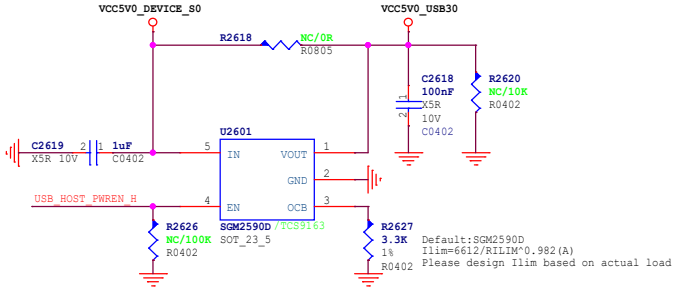
USBHUB_HOST3





USB POWER

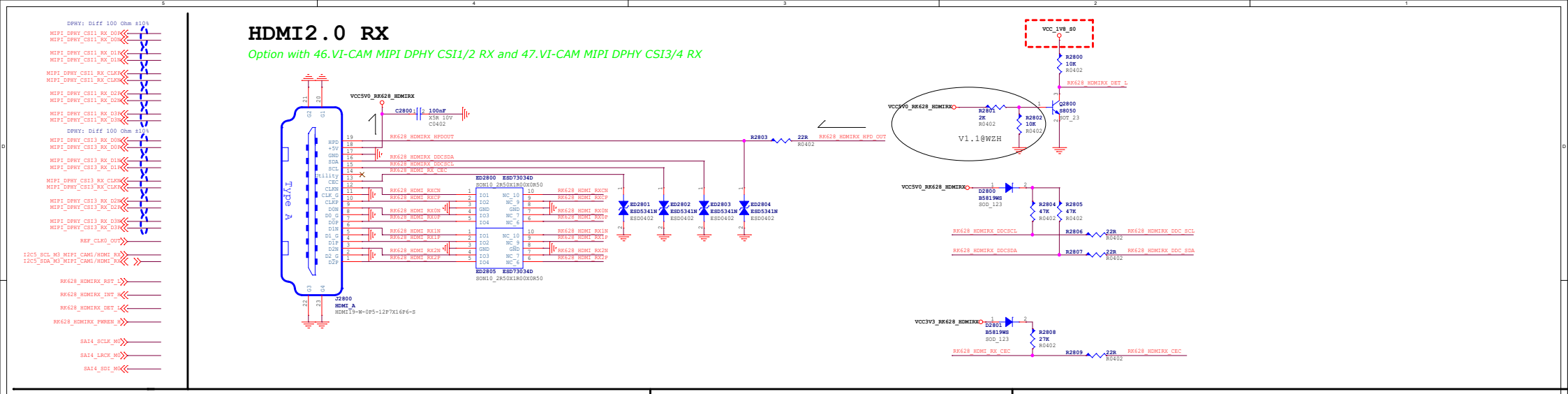


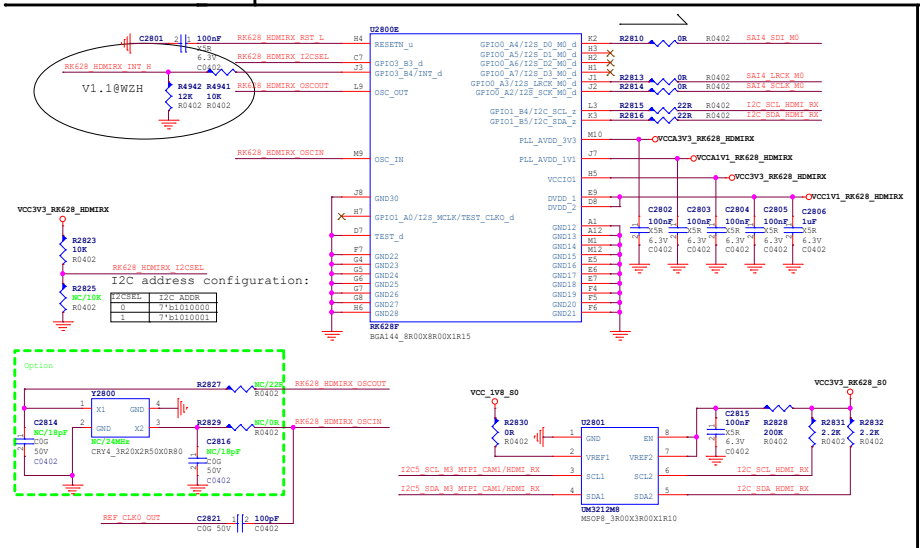


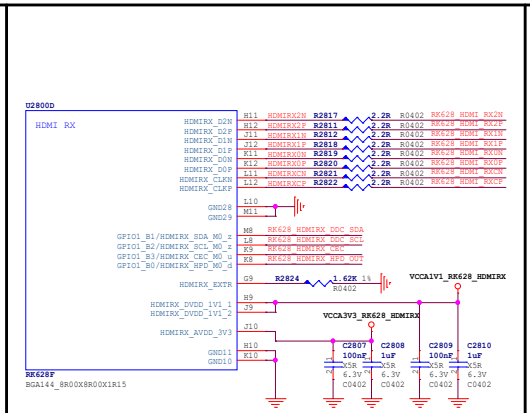
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	26.USB1		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	
Sheet:	27 of 63		

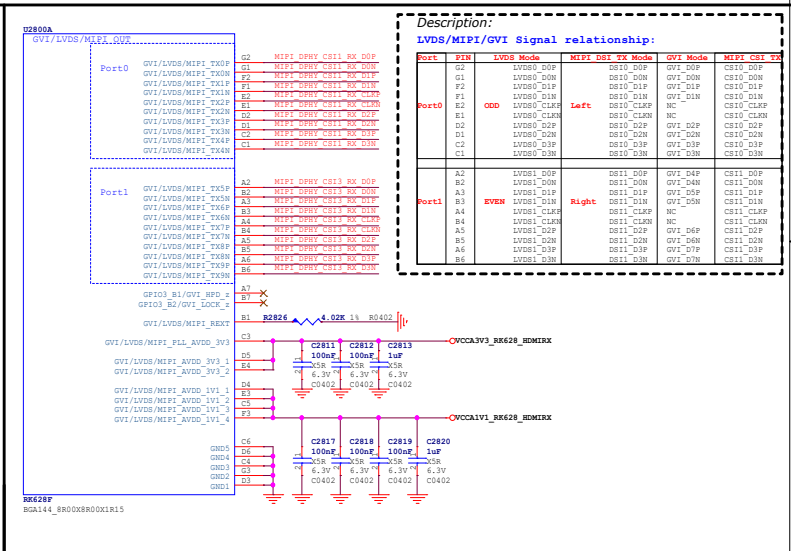
HDMI2.0 RX

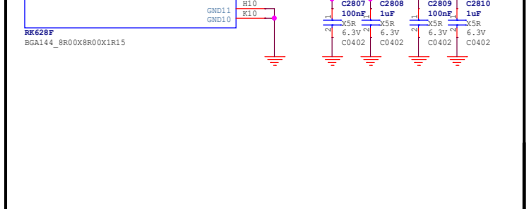
Option with 46.VI-CAM MIPI DPHY CSI1/2 RX and 47.VI-CAM MIPI DPHY CSI3/4 RX

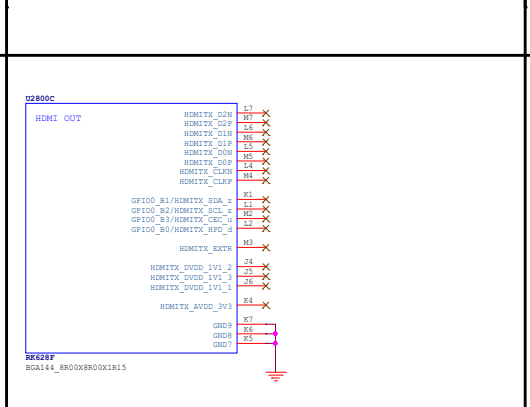


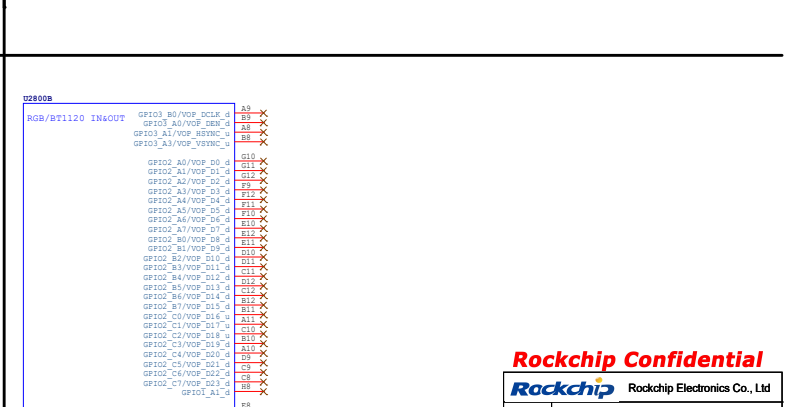












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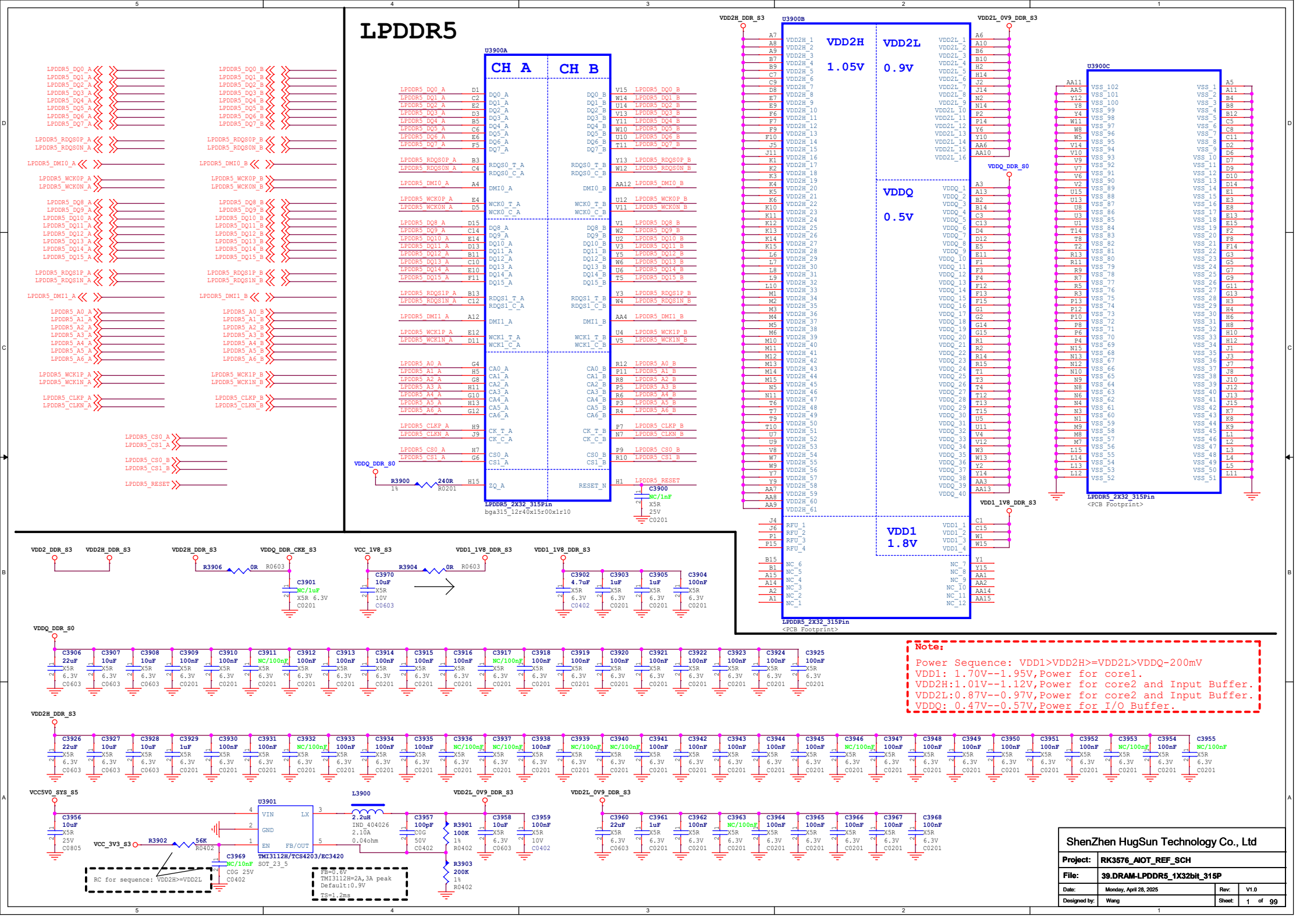
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	28.VI-HDMI20 RX to MIPI RX(Opt)
Date:	Monday, April 28, 2025
Rev:	V1.0
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	37 of 63

LPDDR5



Note:

Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.

ShenZhen HugSun Technology Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	39.DRAM-LPDDR5_1X32bit_315P		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	1 of 99

Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. NC stands for component not mounted temporarily
2. If Value or option is NC, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	01.Index and Notes				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	2 of 63

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2024-03-22	Wesley Huang	1: First version;	

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	02.Revision History				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	3 of 63

Default Power Tree

Note: Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

12V/3A Adapter → VCC12V_DCIN

Note: With PCIe/SATA, the current is estimated according to the actual number of PCIe/SATA

DC/DC 5000mA → VCC5V0_SYS_S5 Seq:0

DC/DC 3000mA → VCC5V0_DEVICE_S0 Seq:5A

DC/DC 3000mA
- Power LED Max:
- PCIe_Slot_3V3 Max:
- PCIe_Slot_12V Max:
- MOS

VCC5V0_DEVICE_S0
- TYPEC 5V Max:
- USB2_HOST 5V Max:
- MIPI DSI LCM 5V Max:
- HDMI TX 5V Max:
- SPK AMP 5V Max:
- Work LED Max:

RK806S-5

		Power on Sequence		
VCC1	BUCK1 6.5A max	Seq:2	VDD_CPU_BIG_S0 Max:	VDD_CPU_BIG_SOC Max:4A
VCC2	BUCK2 5.0A max	Seq:2	VDD_NPU_S0 Max:	VDD_NPU_SOC Max:4A
VCC3	BUCK3 5.0A max	Seq:2	VDD_CPU_LIT_S0 Max:	VDD_CPU_LIT_SOC Max:2A
VCC4	BUCK4 5.0A max	Seq:5	VCC_3V3_S3 Max:	
VCC5	BUCK5 3A max	Seq:2	VDD_GPU_SOC Max:	VDD_GPU_SOC Max:3A
VCC6	BUCK6 3A max	Seq:7	VDDQ_DDR_S0 Max:	LPDDR4x VDDQ / LPDDR5 VDDQ / DDRPHY_CK_VDDQ_SOC / DDRPHY_VDDQ_SOC Max:
VCC7	BUCK7 3A max	Seq:2	VDD_LOGIC_S0 Max:	VDD_LOGIC_SOC Max:1.5A; VDD_LOGIC_MEM_SOC Max:
VCC8	BUCK8 3A max	Seq:3	VCC_1V8_S3 Max:	
VCC9	BUCK9 3A max	Seq:4	VDD2_DDR_S3 Max:	MOS to LPDDR4 VDDQ / LPDDR4/4x VDD2 / LPDDR5 VDD2H / DDRPHY_CKE_VDDQ_SOC Max:
VCC10	BUCK10 3A max	Seq:2	VDD_DDR_S0 Max:	DDRPHY_DVDD_SOC Max:2A
VCC_2V0_PLDO_S3	PLDO1 500mA max	Seq:3	VCCA_1V8_S0	OSC_AVDD1V8_SOC; PLL_AVDD1V8_SOC; SARADC_AVDD1V8_SOC; DDRPHY_PLL_AVDD1V8_SOC; UFS_AVDD1V8_SOC; OSC_UFS_AVDD_SOC; USB3_OTG0/DP_TX_AVDD1V8_SOC; USB2_OTG_AVDD1V8_SOC; MIPI_D/C_PHY_AVDD1V8_SOC; MIPI_CSI1/2_AVDD1V8_SOC; MIPI_CSI3/4_AVDD1V8_SOC; HDMI_TX/eDP_TX_AVDDIO1V8_SOC; HDMI_TX/eDP_TX_AVDDCMN1V8_SOC; PCIE0_SATA0_AVDD1V8_SOC; PCIE1_SATA1_USB3_OTG1_AVDD1V8_SOC Max:
VCC11	PLDO2 300mA max	Seq:3	VCCA1V8_PLDO2_S0	
	PLDO3 300mA max	Seq:4	VDDA_1V2_S0	VCCIO7_VCC_SOC / MIPI_DCPHY_AVDD1V2_SOC Max:
VCC12	PLDO4 500mA max	Seq:5	VCCA_3V3_S0	CODEC VCCA3V3 Max:
	PLDO5 300mA max	Seq:5	VCCIO_SD_S0	VCCIO1_VCC_SOC Max:
VCCA	PLDO6 300mA max	Seq:3	VCCA1V8_PLDO6_S3	VCCA1V8_PLDO6_S3 Max:
	NLDO1 300mA max	Seq:2	VDD_0V75_S3	PMU_LOGIC_DVDD0V75_SOC Max:
VCC_1V1_NLDO_S3	NLDO2 300mA max	Seq:2	VDDA_DDR_PLL_S0	DDRPHY_PLL_DVDD_SOC Max:
VCC13	NLDO3 500mA max	Seq:2	VDDA0V75_HDMI_S0	HDMI_TX/eDP_TX_AVDDD0V75_SOC / HDMI_TX/eDP_TX_AVDDC0V75_SOC Max:
VCC_1V1_NLDO_S3	NLDO4 500mA max	Seq:2	VDDA_0V85_S0	UFS_AVDD0V85_SOC; USB3_OTG0/DP_TX_AVDD0V85_SOC; USB3_OTG0/DP_TX_DVDD0V85_SOC; PCIE0_SATA0_AVDD0V85_SOC; PCIE1_SATA1_USB3_OTG1_AVDD0V85_SOC Max:
VCC14	NLDO5 300mA max	Seq:2	VDDA_0V75_S0	PLL_DVDD0V75_SOC / OTP_DVDD0V75_SOC / USB2_OTG_DVDD0V75_SOC / MIPI_DCPHY_AVDD_SOC / MIPI_CSI1/2_RX_AVDD0V75_SOC / MIPI_CSI3/4_RX_AVDD0V75_SOC Max:
	EXT DC/DC ,2A (VCC_3V3_S3 → EN)	Seq:1	VDD2L_0V9_DDR_S3 Max:	LPDDR5 VDD2L Max:
	EXT DC/DC ,2A (PMIC_EXT_EN_OUT → EN)	Seq:1	VCC_2V0_PLDO_S3 Max:	
	EXT DC/DC ,2A (PMIC_EXT_EN_OUT → EN)	Seq:1	VCC_1V1_NLDO_S3 Max:	
	EXT DC/DC ,2A (VCC_3V3_S0 → EN)	Seq:5B	VCC_UFS_S0 Max:	VCC_UFS_S0(Opt) Max:
	EXT DC/DC ,2A (VCC1V8_UFS_VCCQ2_S0 → EN)	Seq:4B	VCC1V2_UFS_VCCQ_S0 Max:	VCC1V2_UFS_VCCQ_S0(Opt) Max:
	EXT LDO	Seq:0A	VCC3V3_RTC_S5 Max:	RTC_3V3 Max:

LOAD SWITCH VCC_3V3_S0
- Audio ADC ES7202 3V3 Max:
- CODEC ES8388 3V3 Max:
- USB2 HUB Max:
- eMMC_3V3 Max:
- VCC_UFS_S0 Max:
- RGMII PHY0/1 3V3 Max:
- RGMII PHY1 VCCIO Max:
- SPDIF TX/RX Max:
- G-Sensor 3V3 Max:
- VCCIO2_VCC_SOC Max:
- VCCIO4_VCC_SOC Max:
- VCCIO6_VCC_SOC Max:
- USB2_OTG_AVDD3V3_SOC Max:

LOAD SWITCH
- 3 x LDO → SD Card 3V3 Max:
- 3 x LDO → CAM 1V2 Max:
- 3 x LDO → CAM 2V8 Max:
- LOAD SWITCH → CAM 1V8 Max:
- LOAD SWITCH → LCD 3V3 Max:
- CC IC 3V3 Max:
- TP 3V3 Max:
- WIFI BAT Max:
- IR 3V3 Max:
- Debug Uart 3V3 Max:
- PMUIO1_VCC_SOC Max:

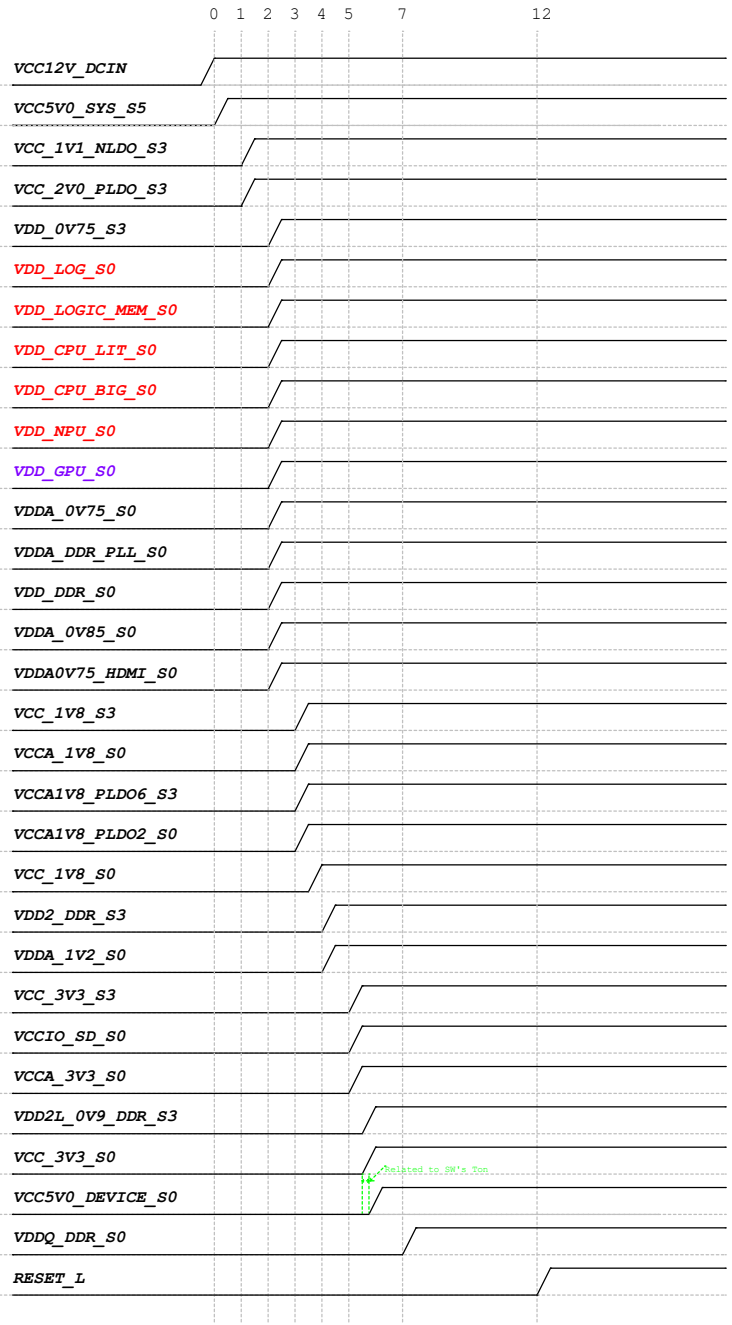
LOAD SWITCH VCC_1V8_S0
- eMMC_1V8 Max:
- VCCIO0_VCC1V8_SOC Max:
- VCCIO5_VCC_SOC Max:

PMOS
- UFS_VCCQ2_1V8_S0 Max:
- LPDDR4/4X VDD1 Max:
- LPDDR5 VDD1 Max:
- WIFI VCCIO Max:
- PMUIO0_VCC1V8_SOC Max:
- VCCIO3_VCC_SOC Max:

Note:
The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	04.Power Tree
Date:	Monday, April 28, 2025
Rev:	V1.0
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	5 of 63

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

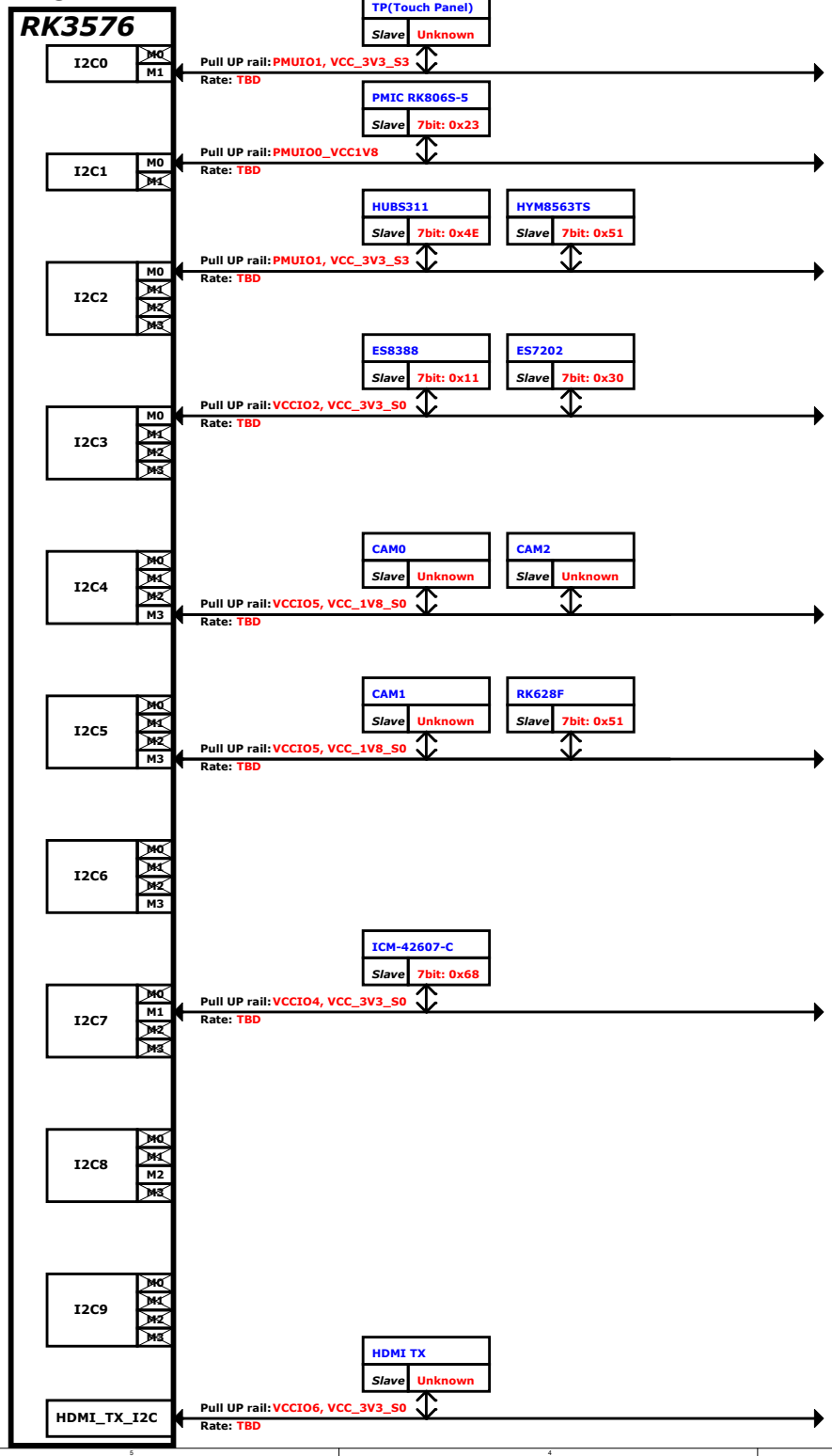
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

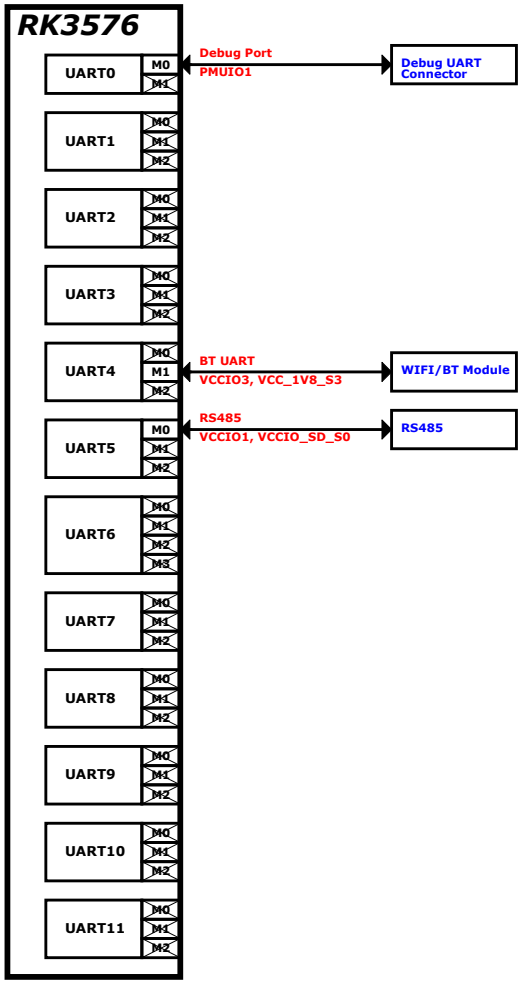
IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	05.Power Sequence and Map				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	6 of 63

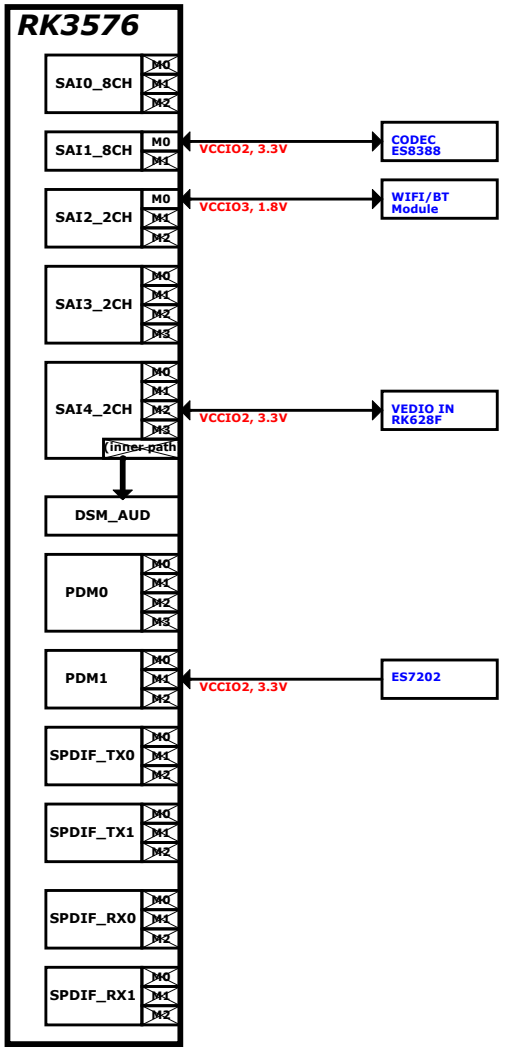
I2C MAP



UART MAP



Audio MAP



Note:

M0 Unselected IOmux path

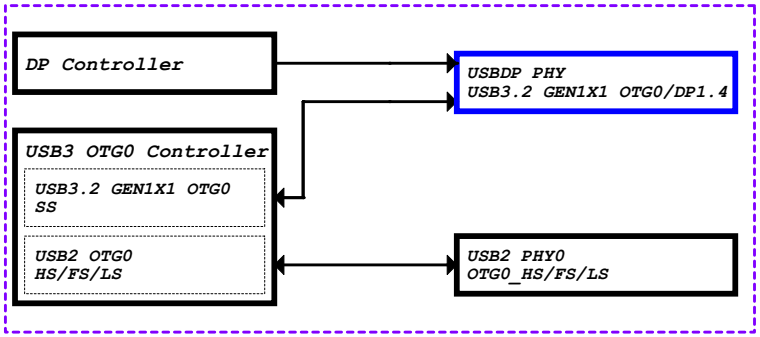
M1 IOmux path in use

At the same time, only one path can be selected.

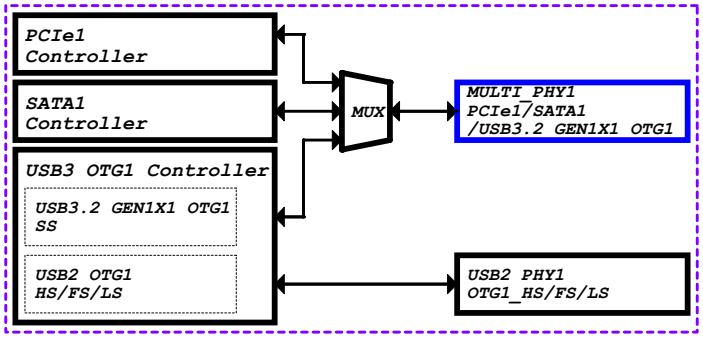
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	05.Lower-Speed Bus Map		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	
		Sheet:	7 of 63

MULTI_PHY Path Map

USBDP PHY--USB3.2 GEN1X1 OTG0/DP1.4



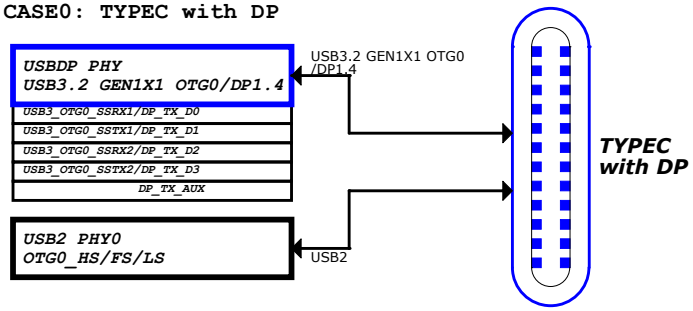
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1



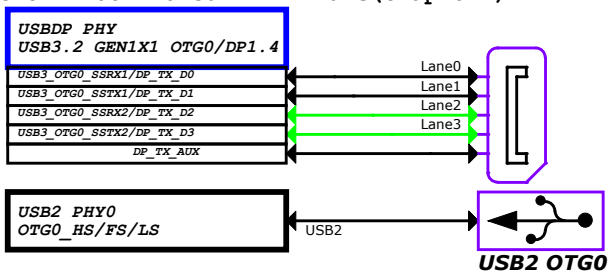
Note:
USB2 OTG1 can only be used when PCIE1/SATA1 is not in use!!!

USB OTG0/DP Application

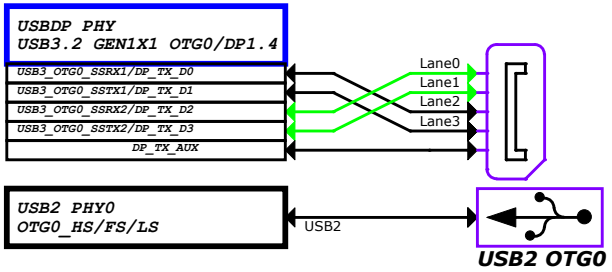
CASE0: TYPEC with DP



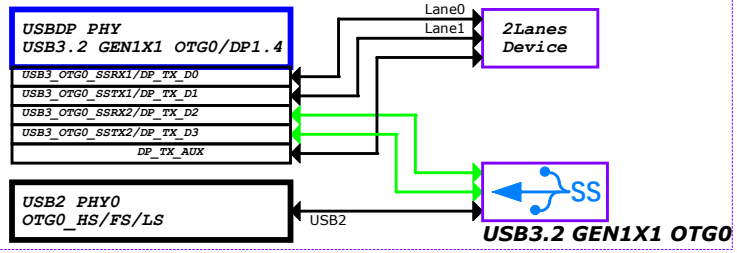
CASE1: USB2 OTG0 + DP 4Lane(Swap OFF)



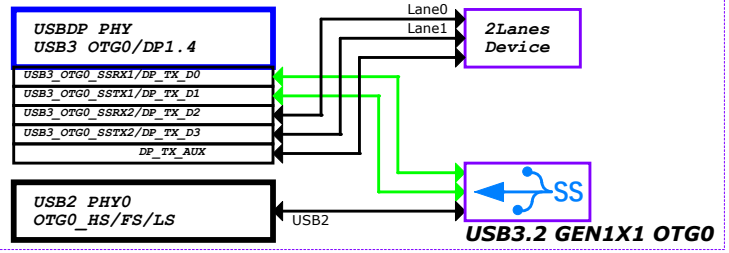
CASE2: USB2 OTG0 + DP 4Lane(Swap ON)



CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap OFF)



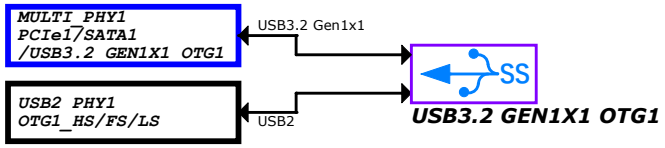
CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap ON)



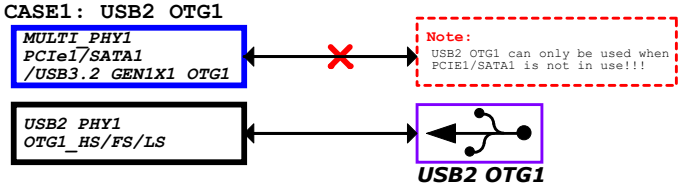
Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

USB OTG1 Application

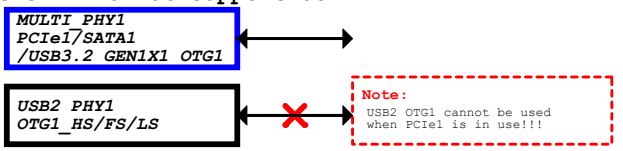
CASE0: USB3.2 GEN1X1 OTG1



CASE1: USB2 OTG1

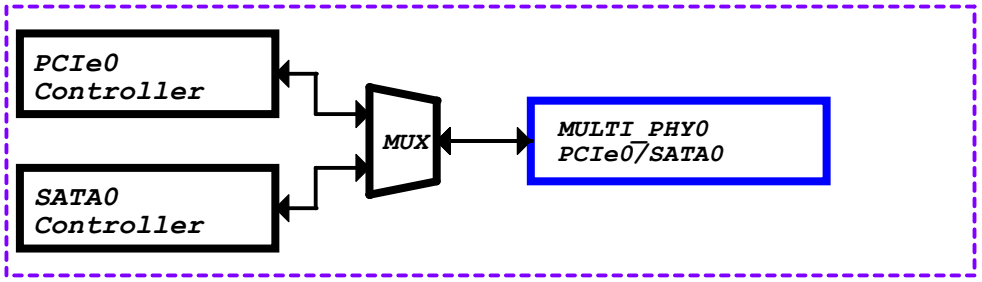


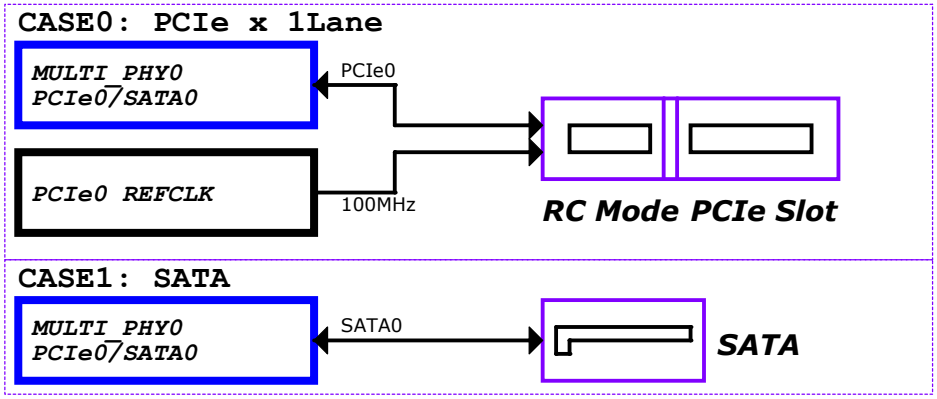
CASE2: Do not support USB



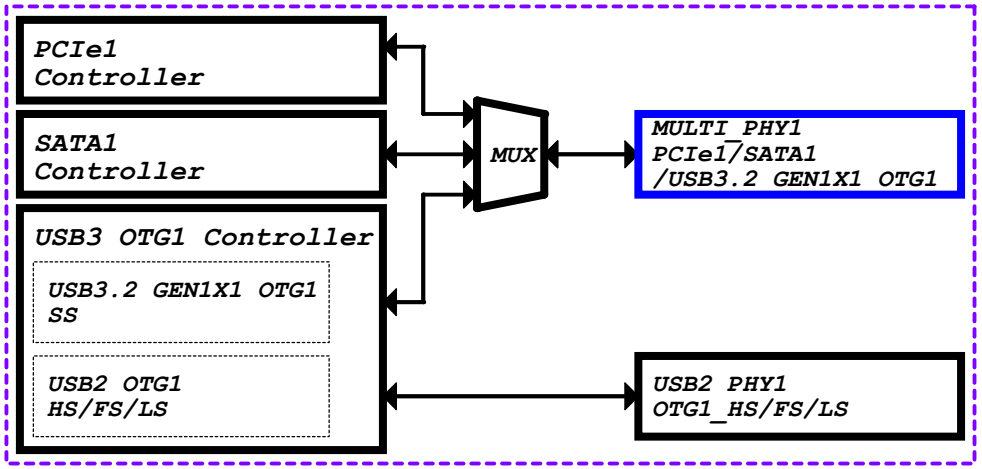
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	07.USB/DP Configure Map
Date:	Monday, April 28, 2025
Rev:	V1.0
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	8 of 63

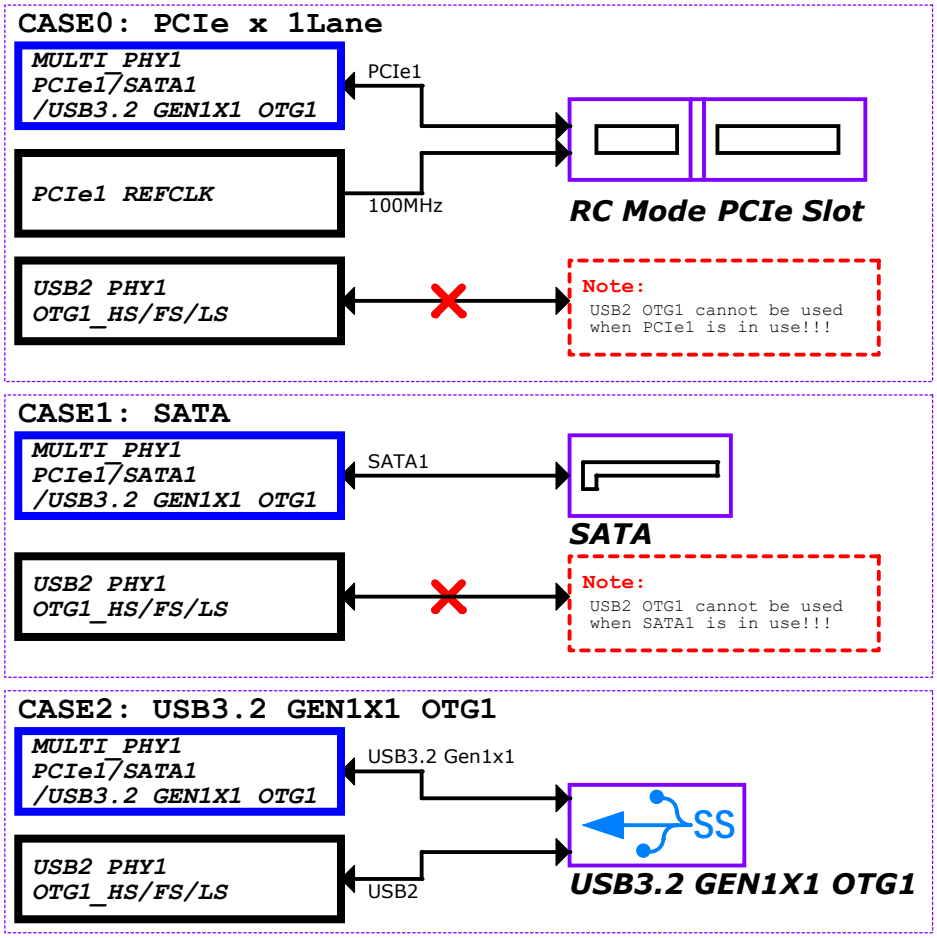
PCIe Combo PHY0--PCIe0/SATA0





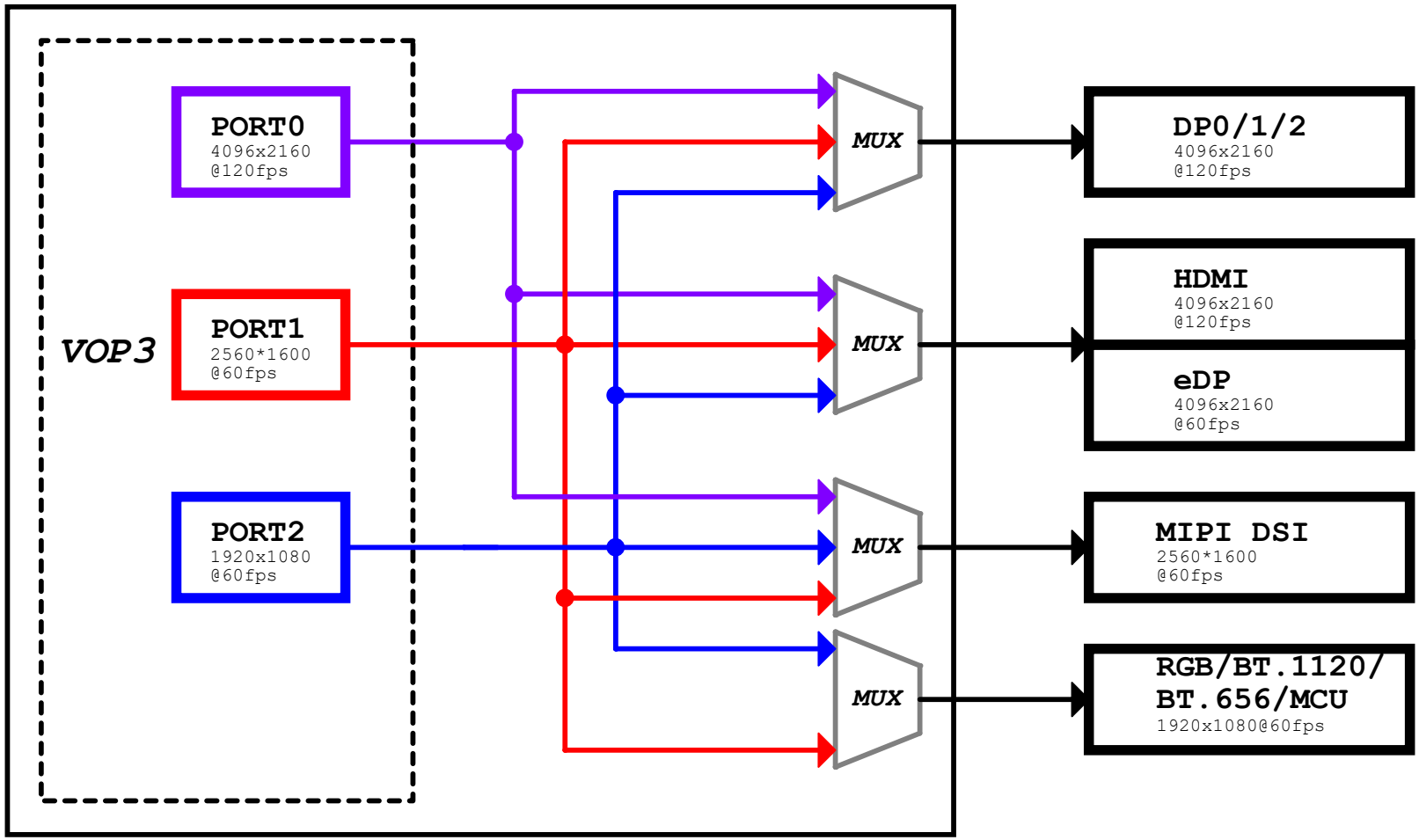
PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1





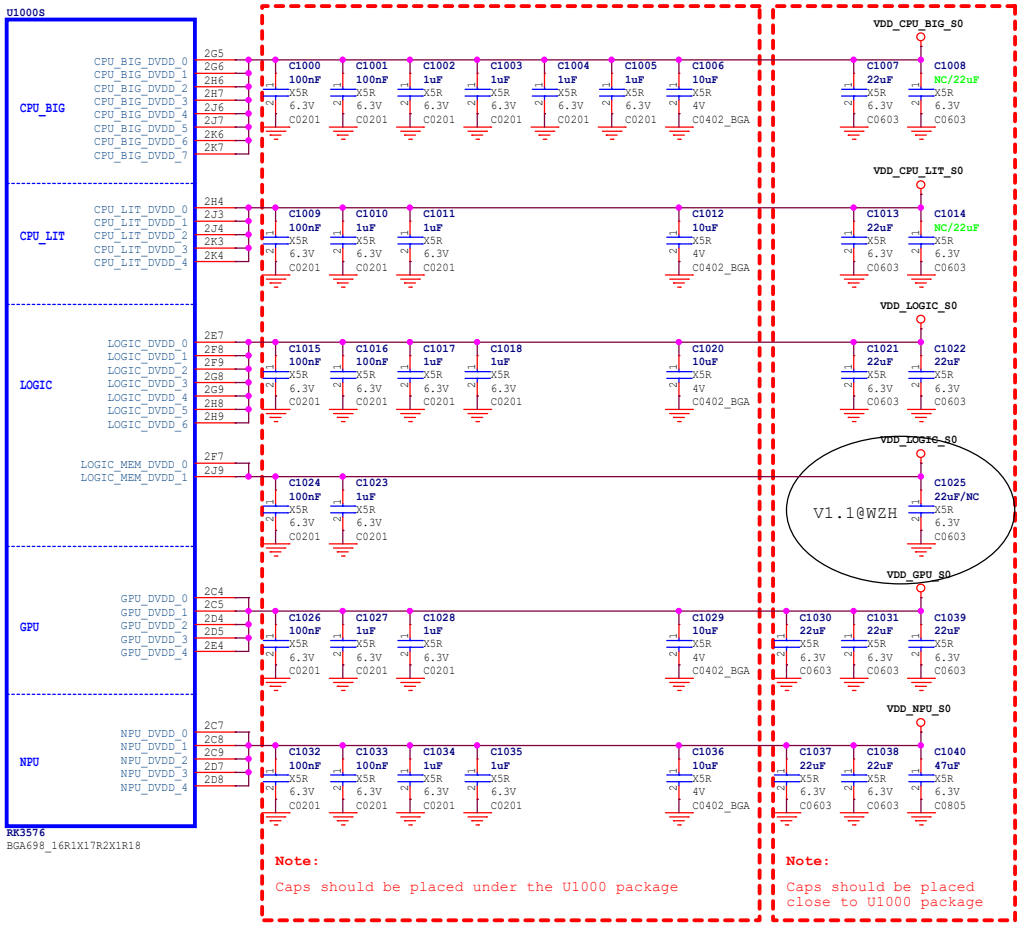
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	08.PCIe Combo PHY Configure Map				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	9 of 63

VO MAP

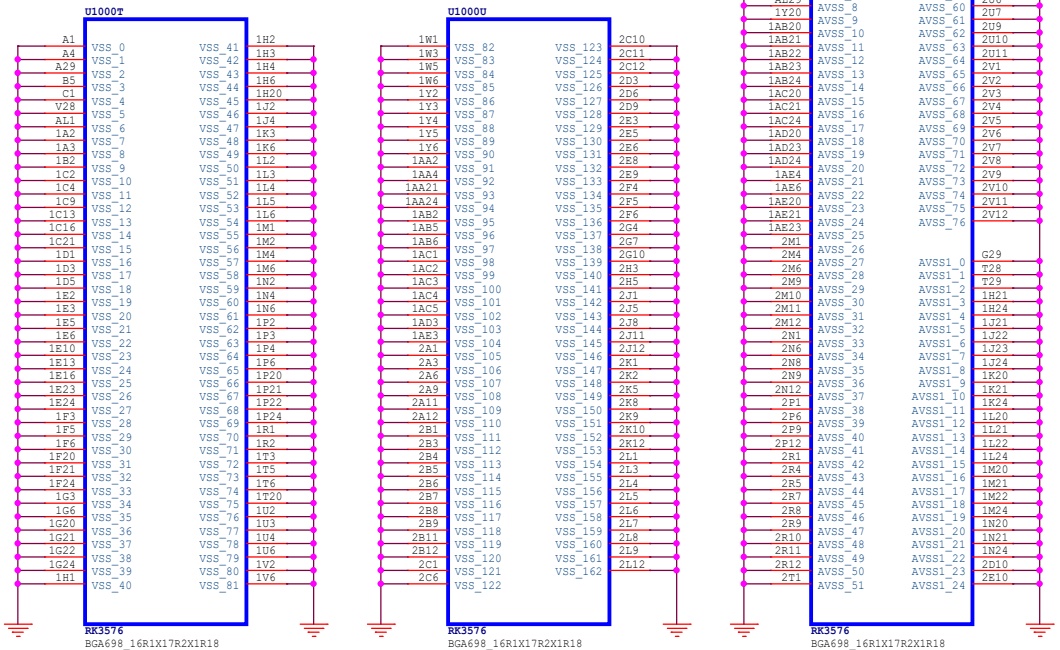


Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	09.VOP Map		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang / Reviewed by:	Sheet:	10 of 63

RK3576_S (Power)



RK3576_T/U/V (GND)



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	10.RK3576-Power/GND				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	11 of 63

RK3576_E (PMUIO0/1)

Note:
Adjust CL1 and CL2 according to the crystal specification
The the load capacitance CL is recommended by the
crystal vendors to obtain target clock frequency.
CL={CL1*CL2/(CL1+CL2))}+PCB strays Total CL<=12pF

U1000E

OSC
- R1100 22R R0402
- Y1100 24MHz
- C1100 CRY4_3R20X2R50X0R80
- C1101 18pF C0G 50V C0402
- R1101 510K R0402
- C1100 18pF C0G 50V C0402
- XOUT_24M U29
- XIN_24M U28
- OSC_XOUT
- OSC_XIN
- OSC_AVDD1V8

VCCA_1V8_S0
- R1119 0R R0402
- C1102 100nF X5R 6.3V C0201
- 2J10

VCCA1V8_PLDO6_S3
- R1124 NC/0R R0201

Option:
Reserved for USB wake-up

PMUI00 Domain
Operating Voltage=1.8V/3.3V

NPOR W28
- C1119 100nF X5R 6.3V C0201 Note: Closed to Pin W28
- R1107 0R R0402
- RESET_L

TVSS 2H10

V29	AUPLL_CLK_IN_M0 /REF_CLK0_OUT /GPIO0_A0_d	REF_CLK0_OUT
1R24	TSADC_CTRL_M0 /GPIO0_A1_z	
1U23	I2C6_SCL_M0 /CLK0_32K_OUT /CLK_32K_IN /GPIO0_A2_d	32KOUT_RTC2SOC
Y28	TSADC_CTRL_M1 /PWR_CTRL1 /GPIO0_A3_d	PMIC_PWR_CTRL1
1T24	PWR_CTRL2 /GPIO0_A4_d	PMIC_PWR_CTRL2
Y29	I2C6_SDA_M0 /PWR_CTRL3 /GPIO0_A5_d	RTC_INT_L
1T21	PMIC_INT /GPIO0_A6_u	PMIC_INT_L
1U21	SPI2_CSN1_M0 /SDMMC0_DETN /GPIO0_A7_u	SDMMC0_DET_L
		C1120 1nF 2 X5R 25V C0201
1U22	I2C0_SCL_M0 /SPI2_CSN0_M0 / AUPLL_CLK_IN_M1/GPIO0_B0_z	WIFI_WAKE_HOST_H
1P23	I2C0_SDA_M0 /SPI2_MISO_M0 /GPIO0_B1_z	BT_WAKE_HOST_H
1T22	I2C1_SCL_M0/ SPI2_CLK_M0 /GPIO0_B2_z	I2C1_SCL_M0_RK806
1T23	I2C1_SDA_M0 / SPI2_MOSI_M0 /GPIO0_B3_z	I2C1_SDA_M0_RK806

PMUI00_VCC1V8 2K11
- C1103 100nF X5R 6.3V C0201
- VCC_1V8_S3

PLL

PMUI01 Domain
Operating Voltage=1.8V/3.3V

AD28	PWM1_CH0_M0 / UART4_TX_M2 / I2C1_SCL_M1 /REF_CLK1_OUT/ GPIO0_B4_d	USBCC_INT_L
AD29	PWM1_CH1_M0 /UART4_RX_M2 /I2C1_SDA_M1 / REF_CLK2_OUT /GPIO0_B5_d	LCD_BL_PWM1_CH1_M0
1Y24	PWM1_CH2_M0 / EDP_TX_HPDIN_M1 / HDMI_TX_HPDIN_M1 /SDMMC1_DETN_M2 /SDMMC0_PWREN/ GPIO0_B6_d	4G_PWREN_H
1W24	PWM1_CH4_M0 /NPU_AVS /UART1_TX_M0 / I2C2_SCL_M0 / / / /GPIO0_B7_d	I2C2_SCL_M0_CC_RTC
AB29	PWM1_CH3_M0 /CPULIT_AVS / UART1_RX_M0 / I2C2_SDA_M0 / / / /GPIO0_C0_d	I2C2_SDA_M0_CC_RTC
AB28	I3C0_SCL_M0 / UART8_TX_M2 /I2C0_SCL_M1 / GPIO0_C1_d	I2C0_SCL_M1_TP
1Y24	I3C0_SDA_M0 /UART8_RX_M2 / I2C0_SDA_M1 / / / / GPIO0_C2_d	I2C0_SDA_M1_TP
1W21	PWM0_CH1_M0 / SPI0_CSN1_M0 /HDMI_TX_CEC_M1 / PDM0_CLK1_M0 / /GPIO0_C3_d	4G_RST
1W22	PWM0_CH0_M0 / UART10_TX_M2 /PDM0_CLK0_M0 /SAI0_MCLK_M1 / /GPIO0_C4_d	PWM0_CH0_M0_IR
1AA22	I3C0_SDA_PU_M0 /UART10_RX_M2 / DP_HPDIN_M1 / /SAI0_SDO0_M1 /GPIO0_C5_d	TP_INT_L
1V21	SPI0_CSN0_M0 / I2C5_SCL_M1 / /SAI0_SCLK_M1/ GPIO0_C6_d	LCD_PWREN_H
1Y23	SPI0_CLK_M0 / I2C5_SDA_M1 /SAI0_LRCK_M1/ GPIO0_C7_d	USB_HOST_PWREN_H
1W23	SPI0_MOSI_M0 / PDM0_SDI0_M0/ SAI0_SDI0_M1/ GPIO0_D0_d	TP_RST_L
AC28	SPI0_MISO_M0 / PDM0_SDI1_M0 / SAI0_SDO3_M1 / SAI0_SDI1_M1/ GPIO0_D1_d	WIFI_PWREN_L
1Y22	UART1_CTSN_M0 /PWM1_CH5_M0 / CPUBIG_AVS / I2C4_SCL_M0 /PDM0_SDI2_M0/SAI0_SDO2_M1 /SAI0_SDI2_M1/GPIO0_D2_d	PCIE0_WAKEn_M0
1AA23	UART1_RTSN_M0 / PWM2_CH0_M0 / GPU_AVS / I2C4_SDA_M0 / PDM0_SDI3_M0 / SAI0_SDO1_M1 / SAI0_SDI3_M1/ GPIO0_D3_d	PCIE0_PWREN_H
1U24	JTAG_TCK_M1 /UART0_TX_M0 / /GPIO0_D4_u	UART0_TX_M0_DEBUG
AA28	JTAG_TMS_M1 /UART0_RX_M0 / /GPIO0_D5_u	UART0_RX_M0_DEBUG

PMUIO1_VCC 1U20
- C1106 100nF X5R 6.3V C0201
- VCC_3V3_S3

PMU_LOGIC_DVDD0V75_0 2L2
PMU_LOGIC_DVDD0V75_1 2L10
- C1107 100nF X5R 6.3V C0201
- C1118 100nF X5R 6.3V C0201
- VDD_0V75_S3

PMUI00/PMUI01/VCCIO7 Domain Logic Power
Operating Voltage=0.75V

RK3576
BGA698_16R1X17R2X1R18

PLL_DVDD0V75 2G11
- C1104 100nF X5R 6.3V C0201
- VDDA_0V75_S0

PLL_AVDD1V8 2H12
- C1105 100nF X5R 6.3V C0201
- VCCA_1V8_S0

PLL_AVSS 2G12

VCC_1V8_S3
- R1105 10K R0402
- R1140 10K R0402
- RESET_L
- RTC_INT_L
- R1121 100K R0402
- SDMMC0_DET_L
- R1127 2.2K R0402
- R1128 2.2K R0402
- I2C1_SDA_M0_RK806
- I2C1_SCL_M0_RK806

VCC_3V3_S3
- R1134 2.2K R0402
- R1135 2.2K R0402
- I2C2_SCL_M0_CC_RTC
- I2C2_SDA_M0_CC_RTC
- R1138 2.2K R0402
- R1139 2.2K R0402
- I2C0_SCL_M1_TP
- I2C0_SDA_M1_TP

RK3576_R (SARADC)

U1000R

SARADC
12-bit 1MS/s

A25	SARADC_IN0_BOOT	Recovery/	C1108 1nF 1 2 X5R 25V C0201
1A22	SARADC_IN1	SARADC_VIN1_KEY/RECOVERY	C1109 1nF 1 2 X5R 25V C0201
1B19	SARADC_IN2	SARADC_VIN2_HW_ID	C1110 1nF 1 2 X5R 25V C0201
1C19	SARADC_IN3	SARADC_VIN3_HP_HOOK	C1111 1nF 1 2 X5R 25V C0201
1E18	SARADC_IN4		C1112 1nF 1 2 X5R 25V C0201
1D19	SARADC_IN5		C1113 1nF 1 2 X5R 25V C0201
1D21	SARADC_IN6		C1114 1nF 1 2 X5R 25V C0201
1E19	SARADC_IN7		C1115 1nF 1 2 X5R 25V C0201

Note:This cap should be placed close to RK3576

Option:
If SARADC_IN4~7 is not used, the filtering capacitor can also be omitted

SARADC_AVDD1V8 2A10
- C1116 100nF X5R 6.3V C0201
- VCCA1V8_PLDO2_S0
- V1.1@WZH

TSADC
TSADC_TEST_OUT_TS 2F10

OTP
OTP_DVDD0V75 2H11
- C1117 100nF X5R 6.3V C0201
- VDDA_0V75_S0

RK3576
BGA698_16R1X17R2X1R18

V1.1@WZH
- VCCA1V8_PLDO2_S0
- R1102 10K 1% R0402
- SARADC_VIN0_BOOT
- R1103 NC R0402

Note:
Closed to RK3576
Stay away from strong interference signals

BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	10K	1.13K	416	FSPI0->USB
Config3	10K	2.49K	816	FSPI1_M0->EMMC->USB
Config4	10K	4.3K	1231	FSPI1_M1->EMMC->USB
Config5	10K	6.8K	1658	FSPI0->UFS->USB
Config6	10K	10K	2048	FSPI1_M0->UFS->USB
Config7	10K	14.7K	2437	UFS->USB
Config8	10K	23.2K	2862	UFS->SDMMC0->USB
Config9	10K	40.2K	3279	RFU
Config10	10K	88.7K	3680	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

V1.1@WZH

Note:
Must be mounted
- VCCA1V8_PLDO2_S0
- R1104 10K 1% R0402
- SARADC_VIN1_KEY/RECOVERY

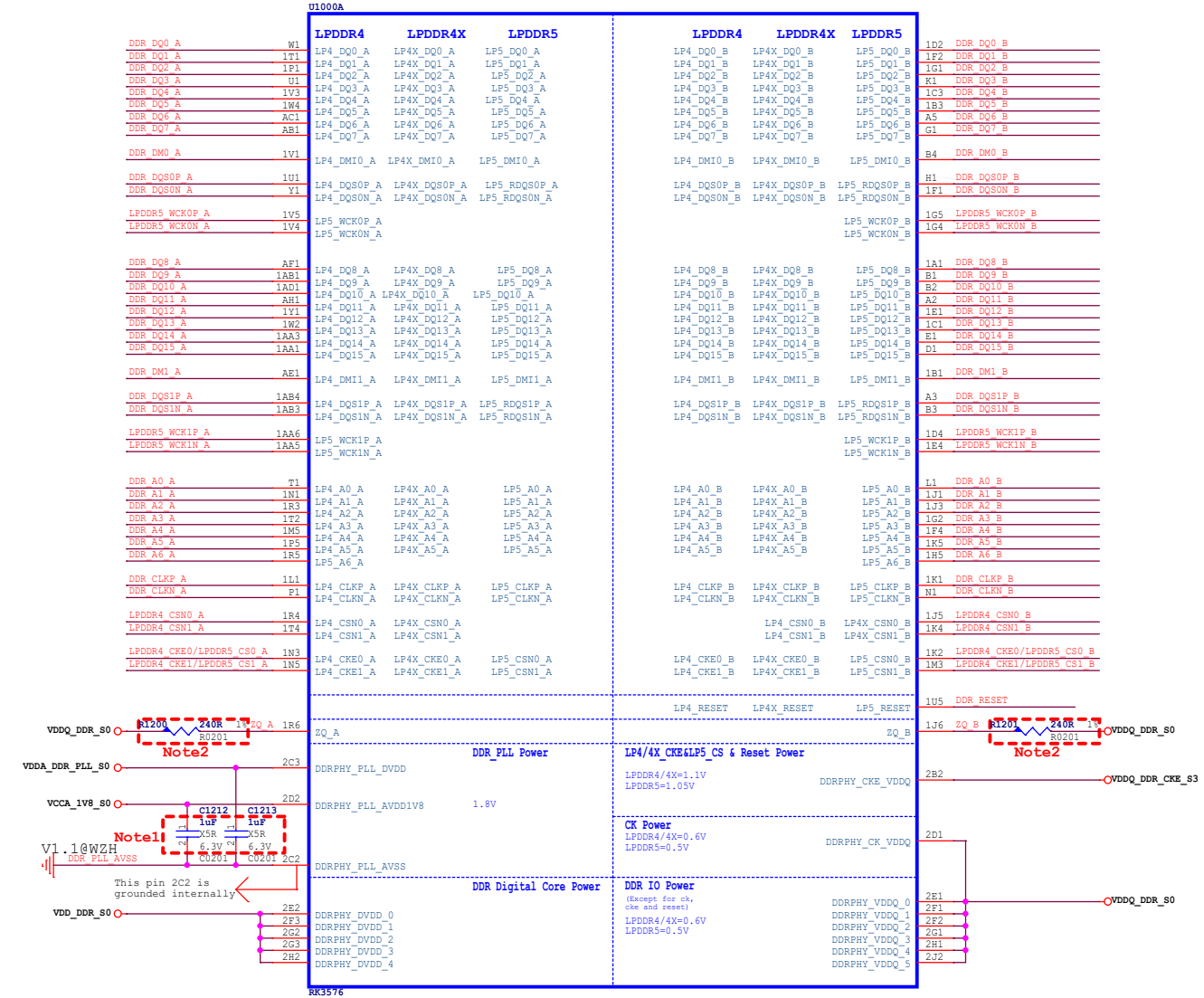
- SARADC_VIN0_BOOT
- SARADC_VIN1_KEY/RECOVERY
- SARADC_VIN2_HW_ID
- SARADC_VIN3_HP_HOOK

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

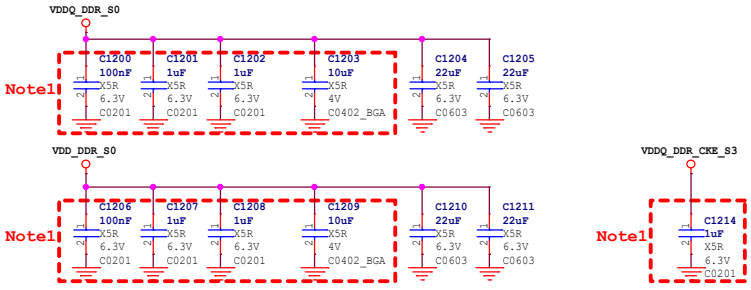
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	11.RK3576-OSC/PLL/PMUIO/SARADC		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet: 12 of 63

RK3576_A(DDRPHY)



DDR FILTER

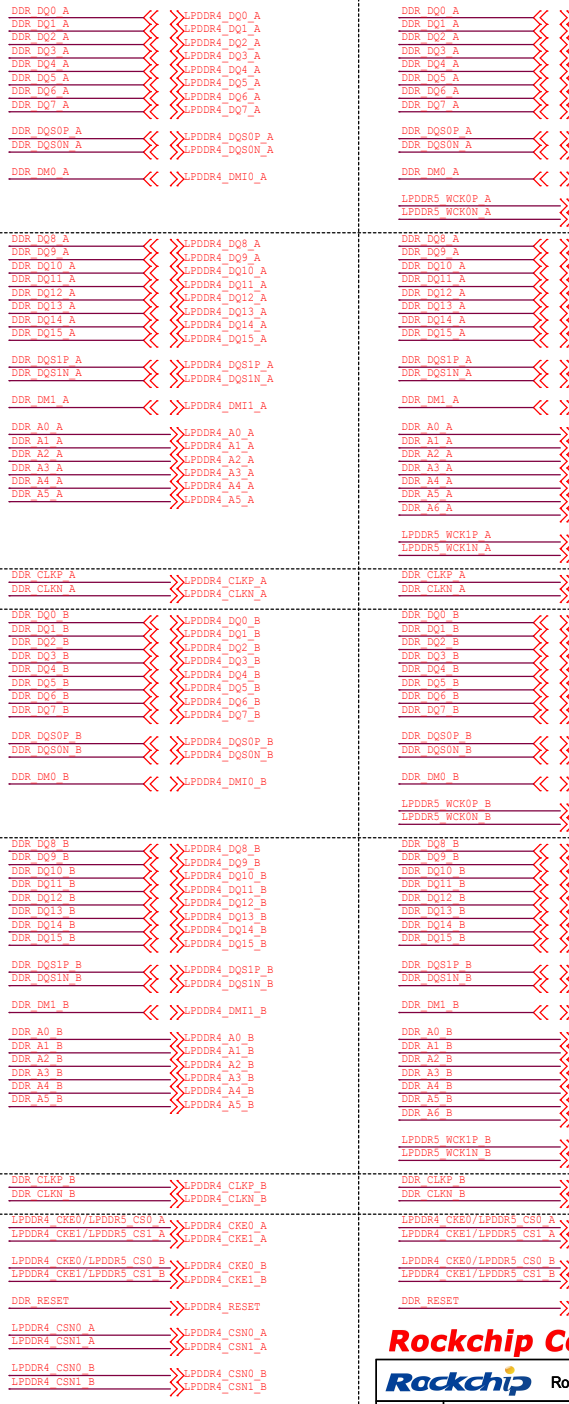


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

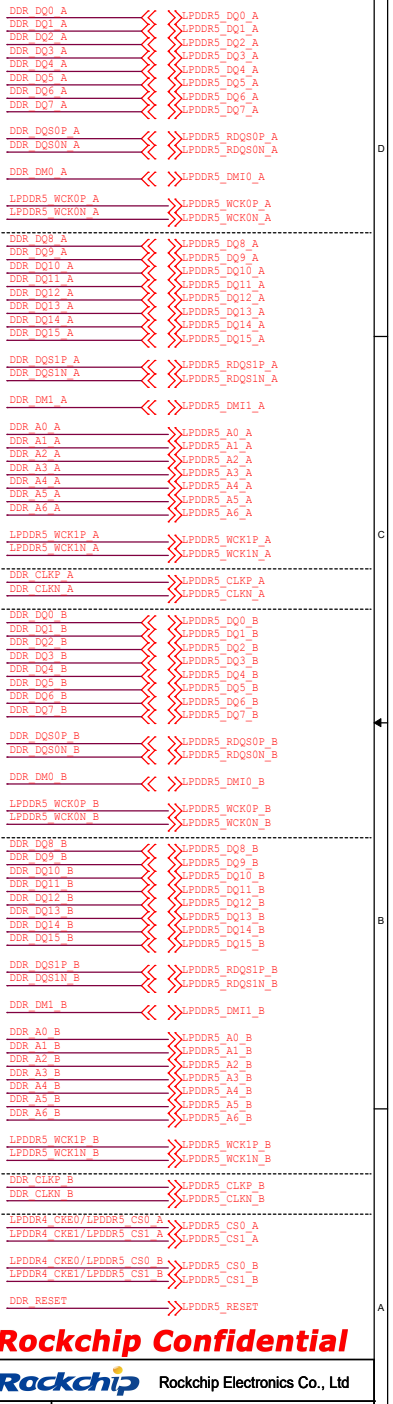
Note1:
Caps in the red line dotted box should be placed under the U1000 package

Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR4/4X



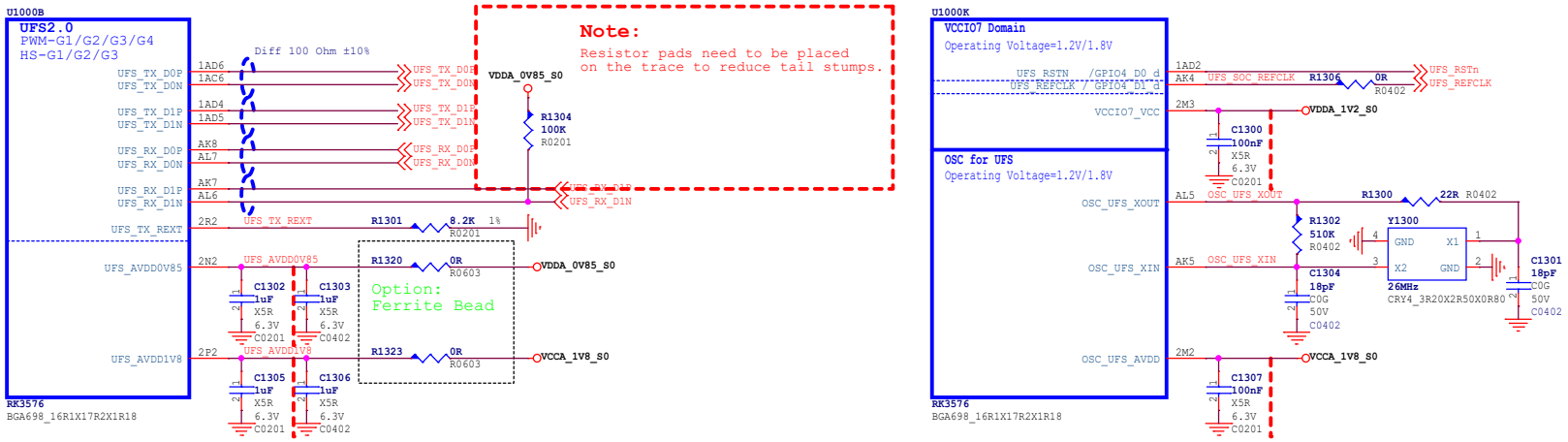
LPDDR5



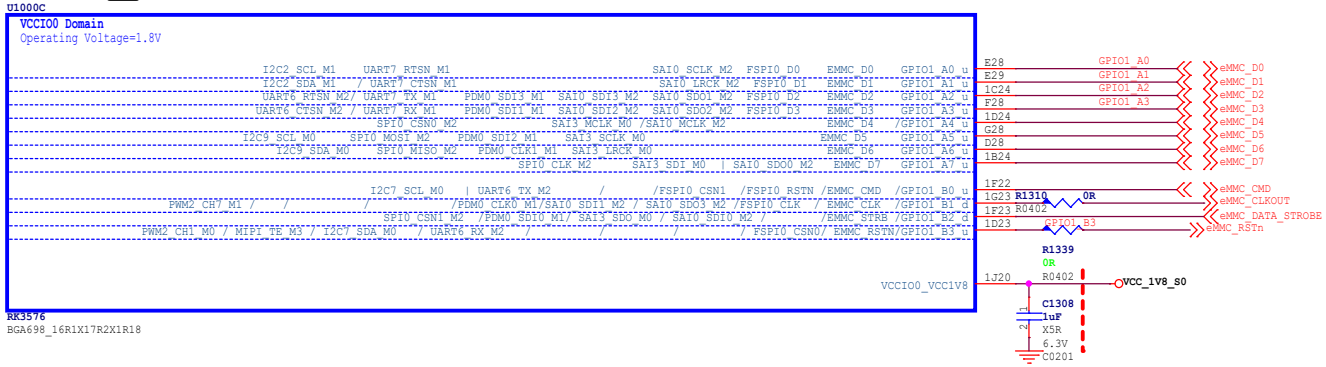
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	12.RK3576-DDR PHY		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet: 13 of 63

RK3576_B (UFS2.1)

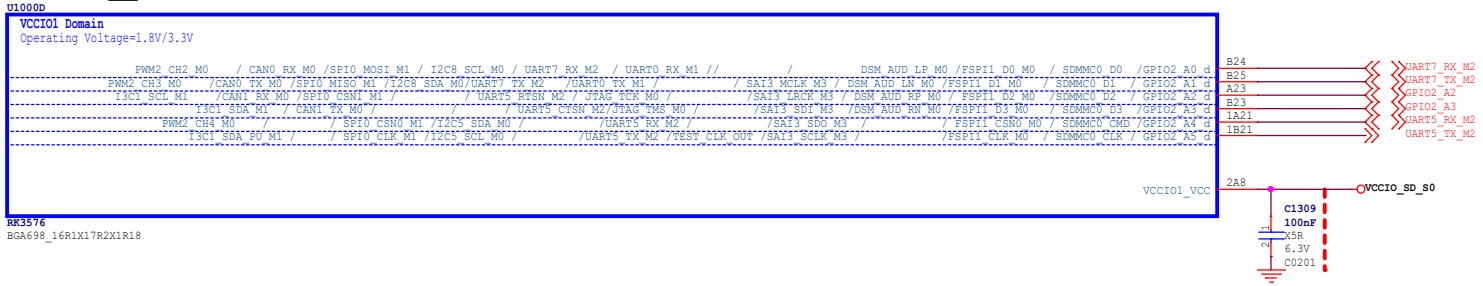


RK3576_C (VCCIO0)



MODE1: EMMC (Default)

RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH			
File:	13.RK3576-eMMC/UFS/SD			
Date:	Monday, April 28, 2025		Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet:	14 of 63

RK3576_L (USB3/DP)

U1000L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

DP_TX_AUXP
DP_TX_AUXN
USB3_OTG0_SSRX1P /DP_TX_D0P
USB3_OTG0_SSRX1N / DP_TX_D0N
USB3_OTG0_SSTX1P / DP_TX_D1P
USB3_OTG0_SSTX1N / DP_TX_D1N
USB3_OTG0_SSRX2P / DP_TX_D2P
USB3_OTG0_SSRX2N / DP_TX_D2N
USB3_OTG0_SSTX2P / DP_TX_D3P
USB3_OTG0_SSTX2N / DP_TX_D3N
USB3_OTG0_REXT / DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85
USB3_OTG0_DP_TX_DVDD0V85
USB3_OTG0_DP_TX_AVDD1V8

RK3576
BGA698_16R1X17R2X1R18

Support: Type-C With Displayport Alternate Mode

Diff 100 Ohm ±10%
2T2 DP_TX_AUXP
2T3 DP_TX_AUXN

Diff 95 Ohm ±10%
AK10 USB3_OTG0_SSRX1P/DP_TX_D0P
AL10 USB3_OTG0_SSRX1N/DP_TX_D0N
AL11 USB3_OTG0_SSTX1P/DP_TX_D1P
AK11 USB3_OTG0_SSTX1N/DP_TX_D1N
AK12 USB3_OTG0_SSRX2P/DP_TX_D2P
AL12 USB3_OTG0_SSRX2N/DP_TX_D2N
AL13 USB3_OTG0_SSTX2P/DP_TX_D3P
AK13 USB3_OTG0_SSTX2N/DP_TX_D3N

R1400 8.2K 1% R0201
2T7 USB3_OTG0_DP_TX_REXT

2M5 2N5 VDDA_0V85_S0
C1400 1uF X5R 6.3V C0201
C1401 NC/1uF X5R 6.3V C0402

2N4 VCCA_1V8_S0
C1402 1uF X5R 6.3V C0201
C1403 NC/1uF X5R 6.3V C0402

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Note: If using the DP interface to light up the eDP screen, there may be compatibility issues. Please consult RK for detail.

RK3576_M (USB2)

U1000M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP
USB2_OTG0_DM
USB2_OTG0_ID
USB2_OTG0_VBUSDET
USB2_OTG0_REXT

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP
USB2_OTG1_DM
USB2_OTG1_ID
USB2_OTG1_VBUSDET
USB2_OTG1_REXT
USB2_OTG_DVDD0V75
USB2_OTG_AVDD1V8
USB2_OTG_AVDD3V3

RK3576
BGA698_16R1X17R2X1R18

Diff 90 Ohm ±10%
AK9 USB2_OTG0_DP
AL9 USB2_OTG0_DM

2R6 Note: There is an internal pull-up resistor connected to 1.8V
USB2_OTG0_ID

2P3 USB2_OTG0_VBUSDET

2R3 USB2_OTG_REXT R1401 200R 1% R0402
C1404 100nF X5R 10V C0402

Diff 90 Ohm ±10%
2T4 USB2_HOST1_DP
2T5 USB2_HOST1_DM

2T9
2T10

2U8 USB2_OTG1_REXT R1402 200R 1% R0402

2P5 USB2_OTG_DVDD0V75 VDDA_0V75_S0
C1405 100nF X5R 6.3V C0201

2P4 USB2_OTG_AVDD1V8 VCCA_1V8_S0
C1406 100nF X5R 6.3V C0201
C1407 NC/1uF X5R 6.3V C0402

2P7 USB2_OTG_AVDD3V3 VCC_3V3_S0
C1408 100nF X5R 6.3V C0201

Note!!!
The USB2 OTG1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

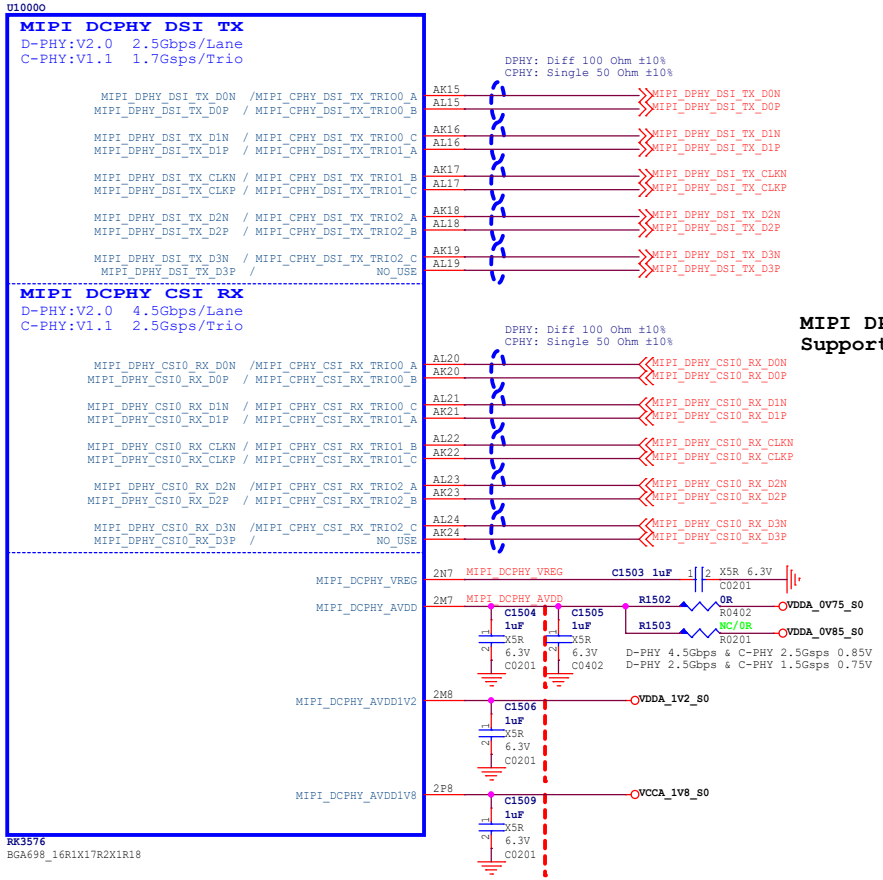
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Reserved for test
USB wakes up SOC

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	14.RK3576-TypeC/USB		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by: Wesley Huang	Reviewed by:	Sheet:	15 of 63

RK3576_O(MIPI DCPHY)

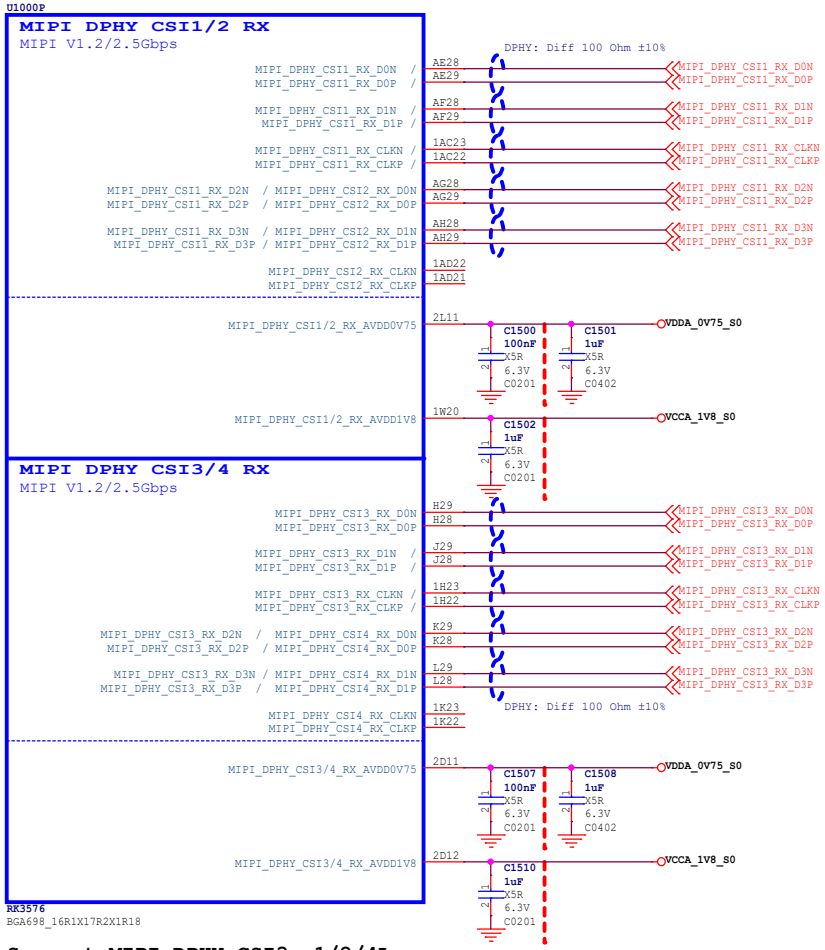


MIPI DPHY CSI0:
Support 1/2/4Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

Support MIPI DPHY CSI1: 1/2/4Lane
Support MIPI DPHY CSI2: 1/2Lane
Support: MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane



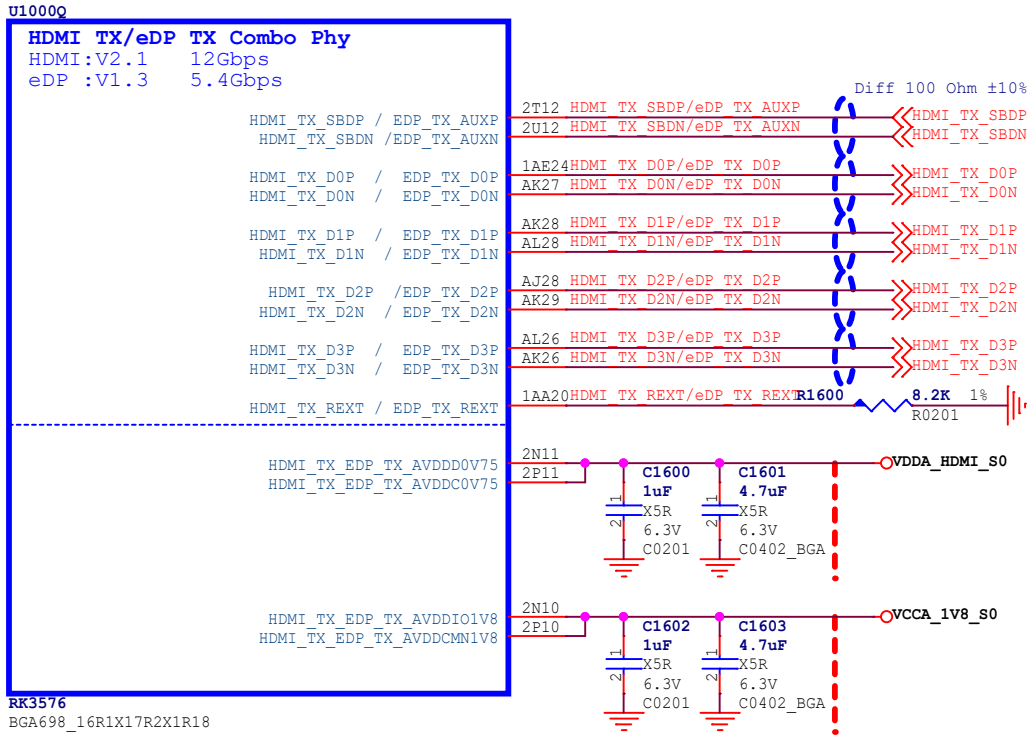
Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI3 2Lane + MIPI DPHY CSI4 2Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	15.RK3576-MIPI DSI/CSI				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	16 of 63

RK3576_Q(HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz

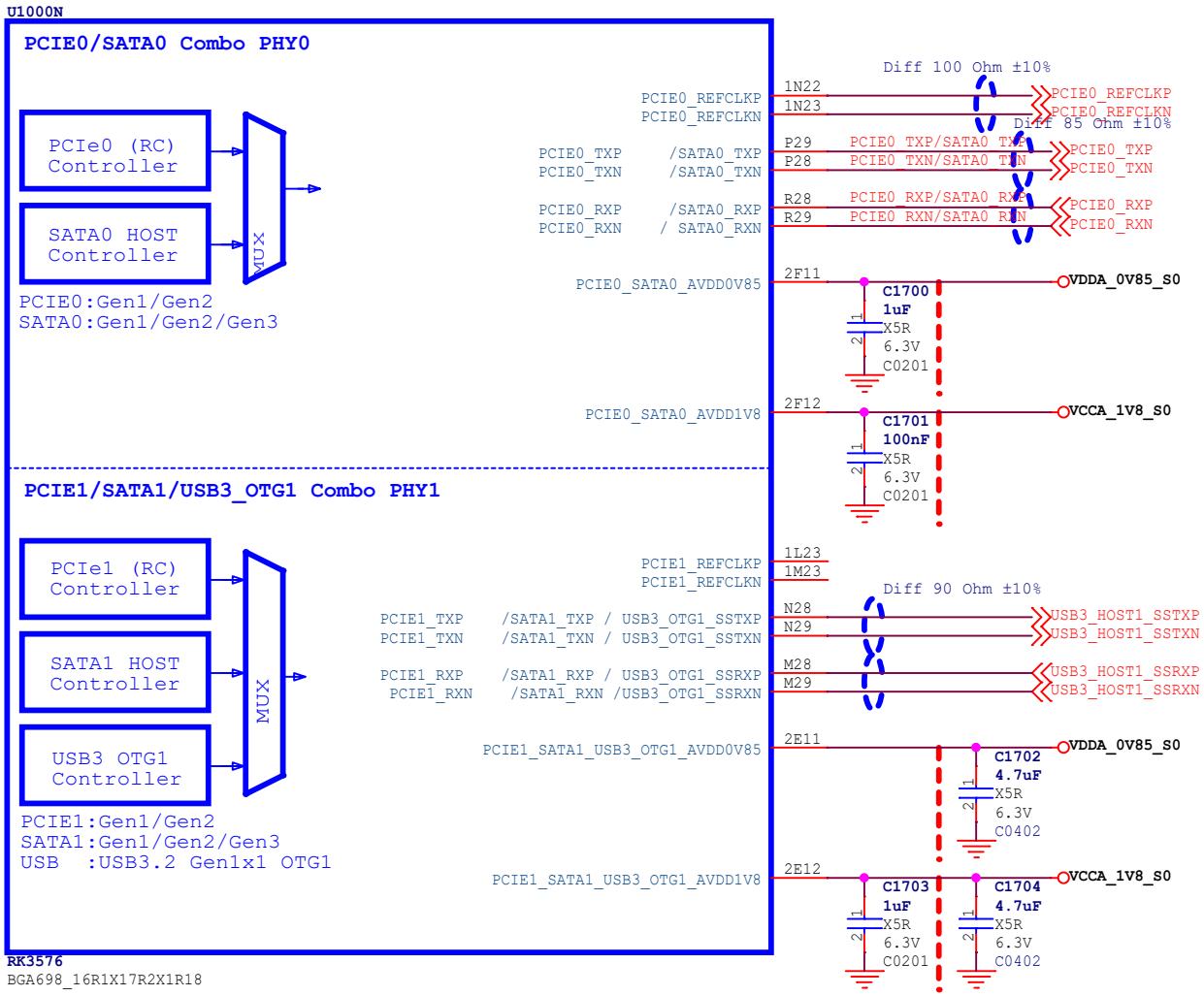


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	16.RK3576-HDMI/eDP		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by: Wesley Huang	Reviewed by:	Sheet:	17 of 63

RK3576_N(PCIe/SATA/USB3)



Note!!!

If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 OTG1 function cannot be used

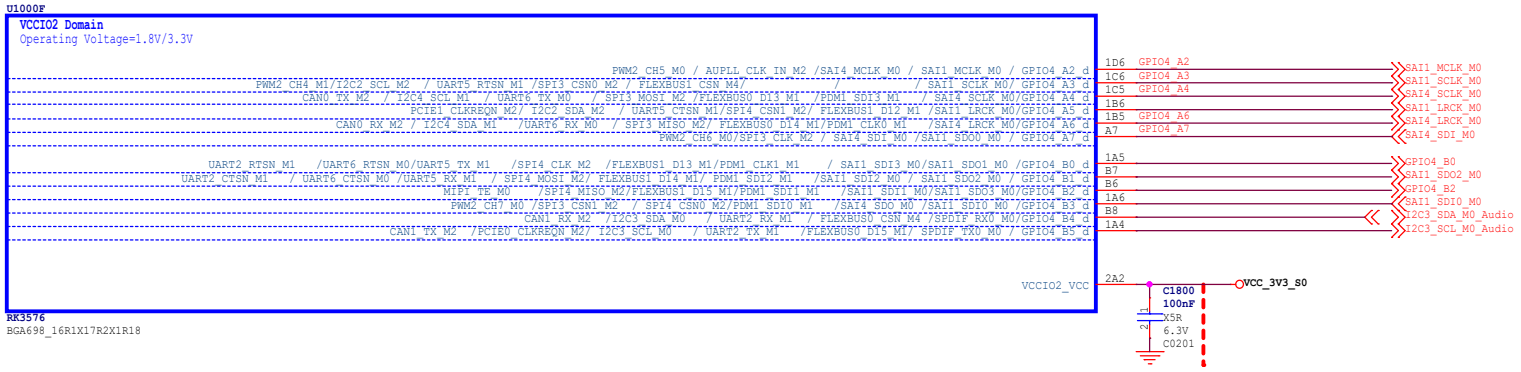
Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

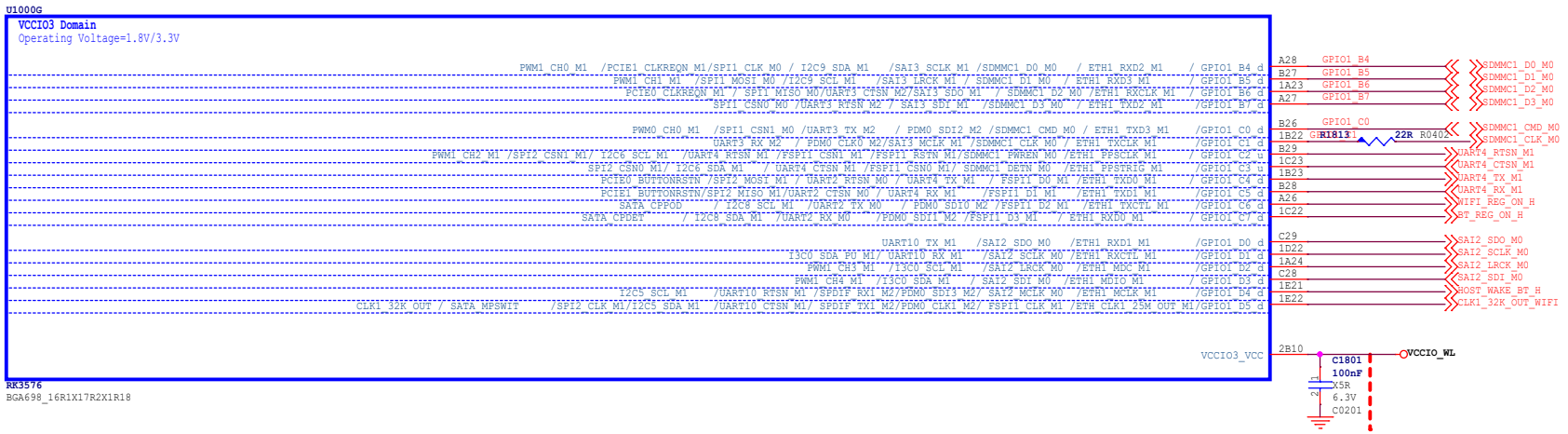
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	17.RK3576-PCIe/SATA/USB3		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by: Wesley Huang	Reviewed by:	Sheet:	18 of 63

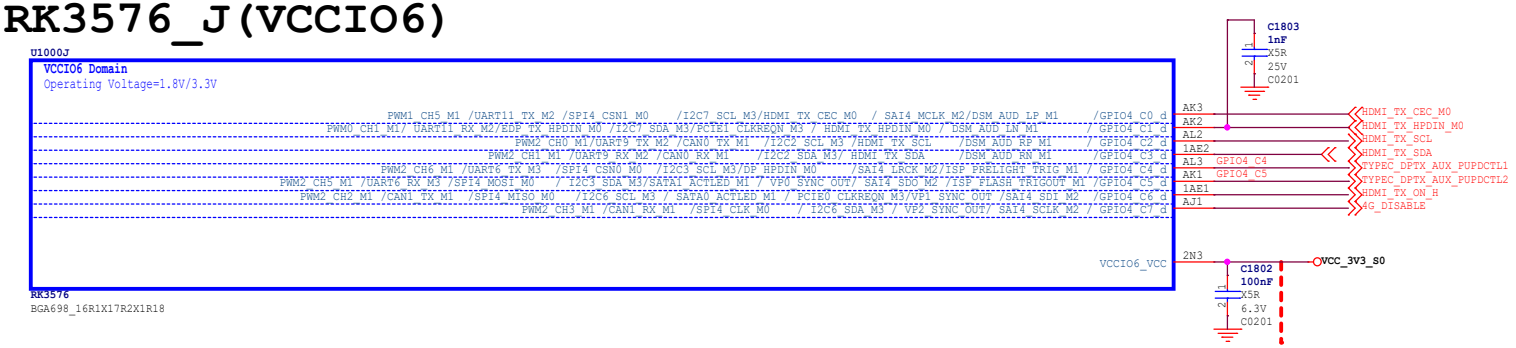
RK3576_F(VCCIO2)



RK3576_G(VCCIO3)



RK3576_J(VCCIO6)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	18.RK3576-GPIO VCCIO2/3/6		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang / Reviewed by:	Sheet:	19 of 63

RK3576_H(VCCIO4)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

RK3576

BGA698_16R1X17R2X1R18

VCC_3V3_S0

R1954 2.2K R0402

SIM_DET

SPK_CTL_H

SPDIF_TX1_M1

VCCIO4_VCC

C1900 NC/100nF X5R 6.3V C0201

C1901 1uF X5R 6.3V C0201

RK3576_I(VCCIO5)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

RK3576

BGA698_16R1X17R2X1R18

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

VCCIO5_VCC_0

VCCIO5_VCC_1

C1902 NC/100nF X5R 6.3V C0201

C1903 1uF X5R 6.3V C0201

VCC_1V8_S0

R1926 2.2K R0402

R1927 2.2K R0402

R1934 2.2K R0402

R1935 2.2K R0402

I2C4_SDA_M3_MIPI_CAM0

I2C4_SCL_M3_MIPI_CAM0

I2C5_SDA_M3_MIPI_CAM1/HDMI_RX

I2C5_SCL_M3_MIPI_CAM1/HDMI_RX

MIPI_DPHY_CSI_CAM2_PWREN_H

MIPI_DPHY_CSI_CAM0_PWREN_H

MIPI_DPHY_CSI_CAM2_PDN_H

MIPI_DPHY_CSI_CAM0_RST_H

MIPI_DPHY_CSI_CAM0_CLKOUT

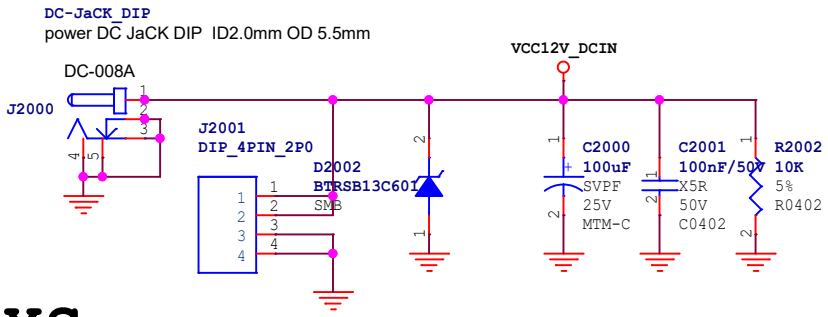
MIPI_DPHY_CSI_CAM2_CLKOUT

Rockchip Confidential

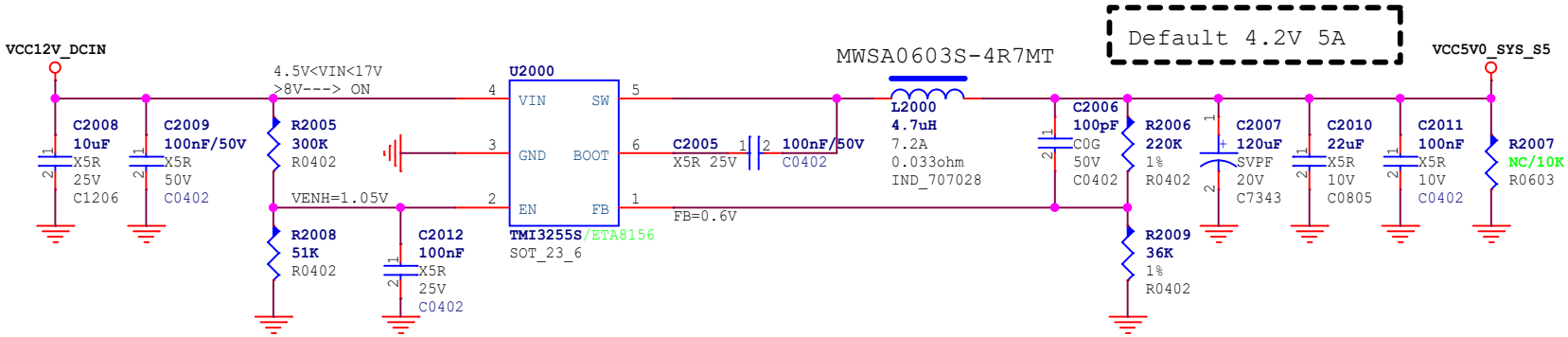
Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	19.RK3576-GPIO VCCIO4/5		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet: 20 of 63

12V/3A DCIN

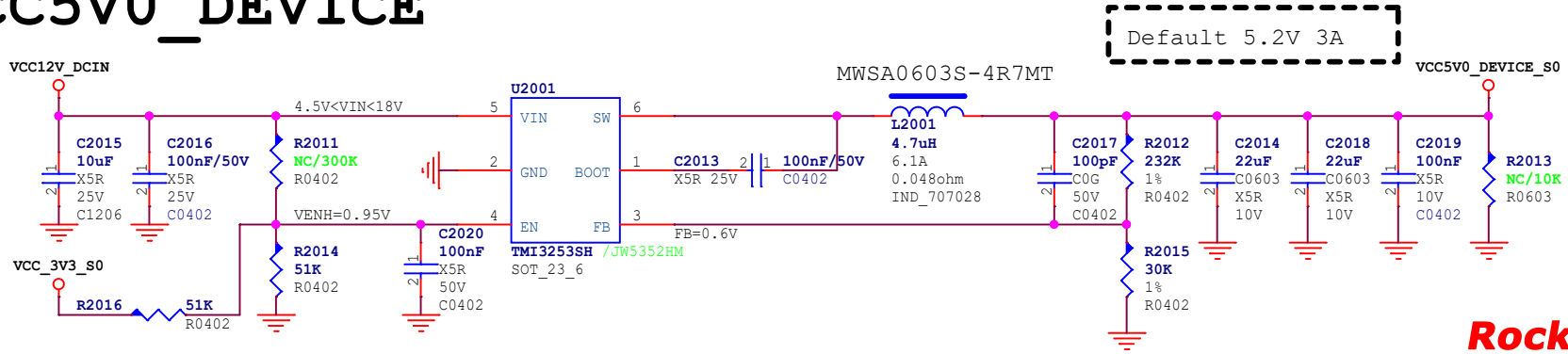
Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe



VCC5V0_SYS



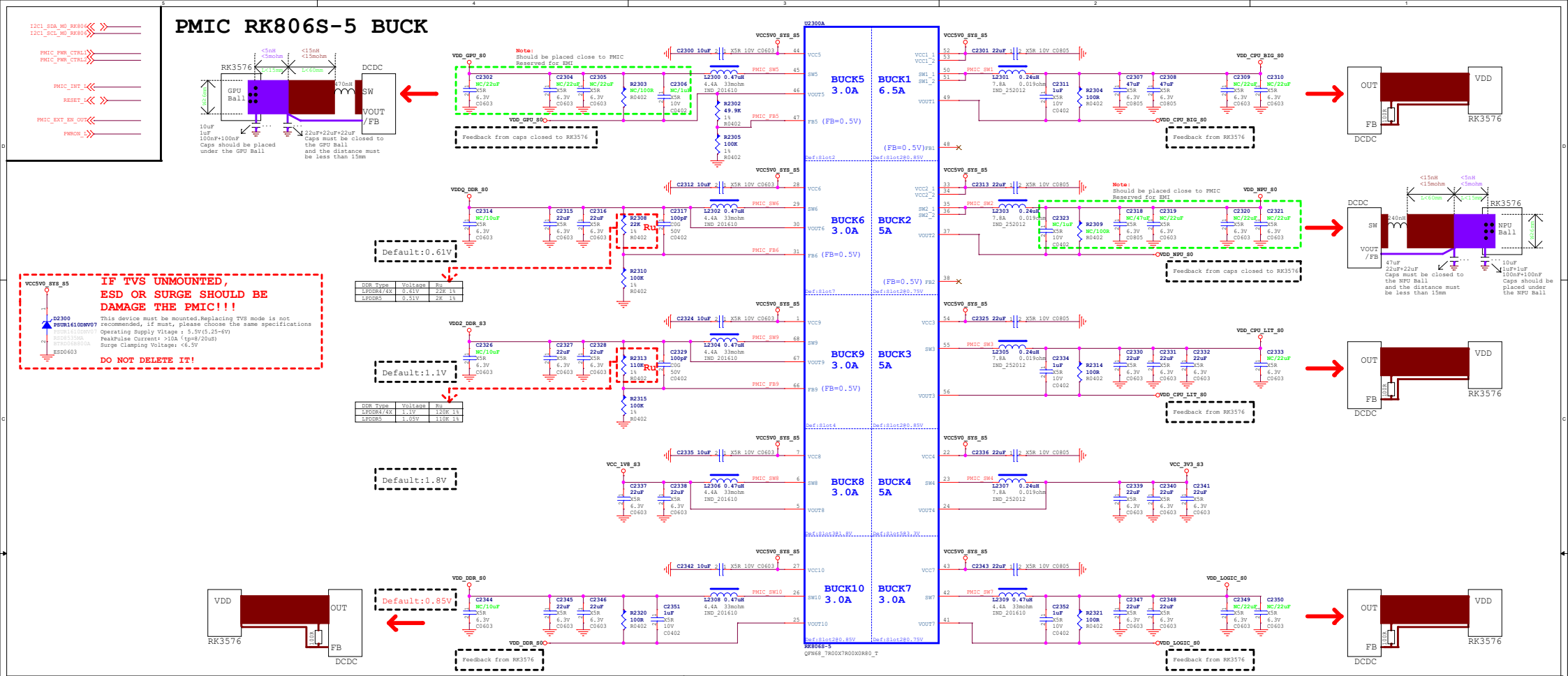
VCC5V0_DEVICE



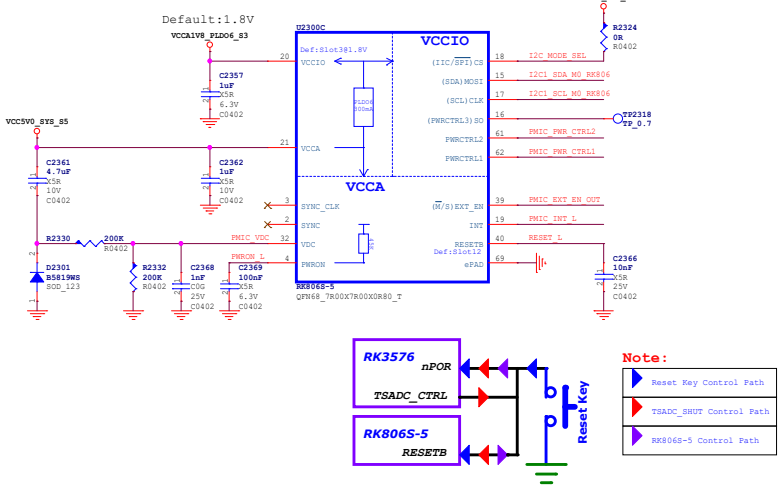
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	20.Power-DC IN		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by: Wesley Huang	Reviewed by:	Sheet:	21 of 63

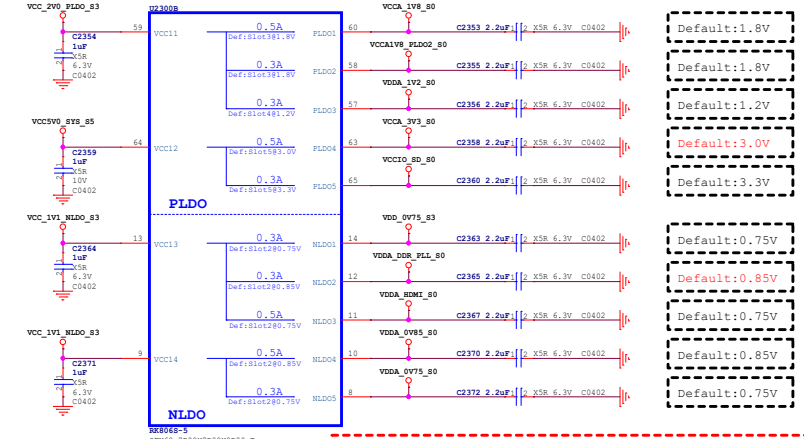
PMIC RK806S-5 BUCK



PMIC RK806S-5 Managerment



PMIC RK806S-5 LDO

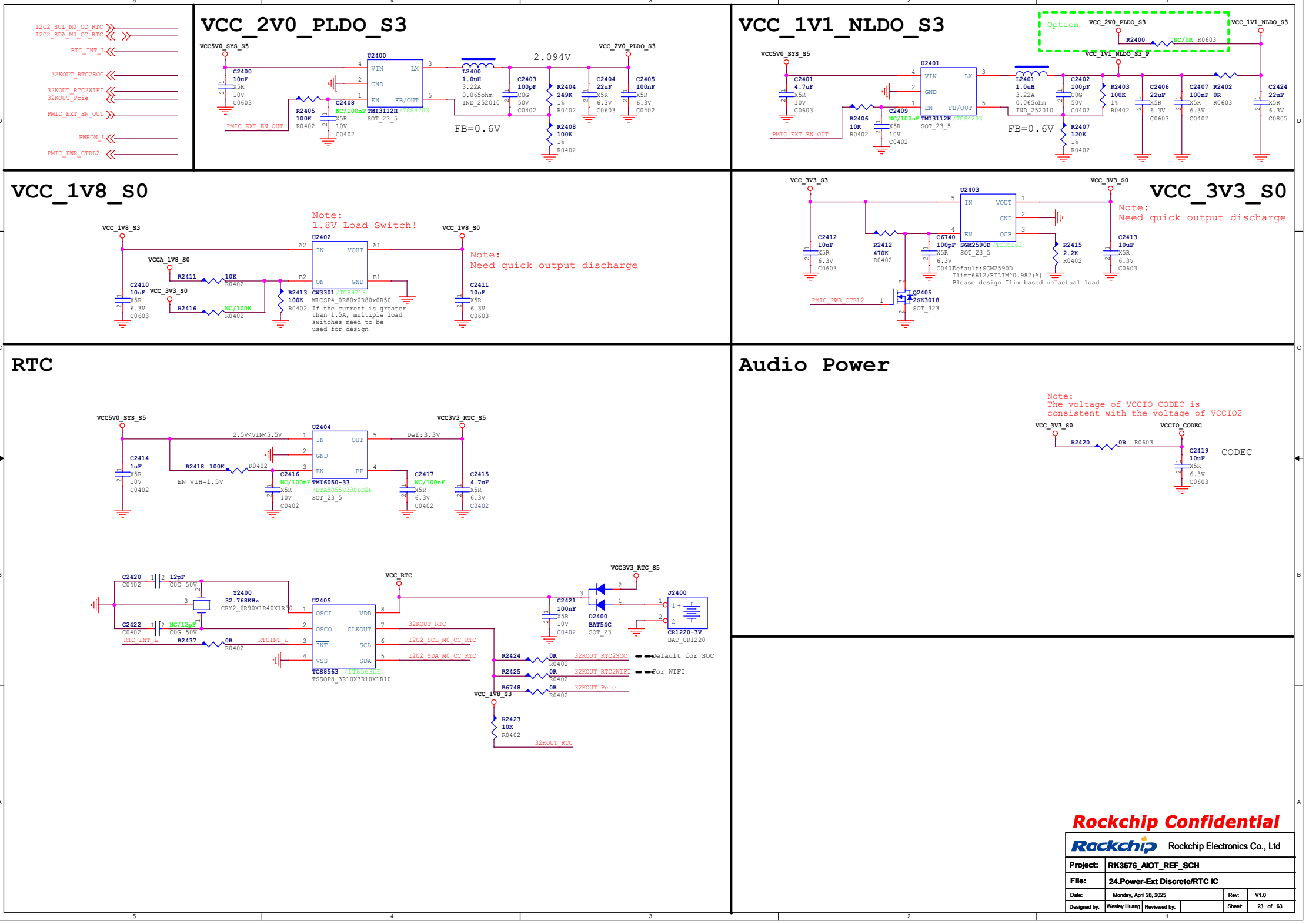


Note:

The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	23.Power-PMIC RK806S-5
Date:	Monday, April 28, 2025
Rev:	V1.0
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	22 of 63


I2C2_SCL_M0_CC_RTC
I2C2_SDA_M0_CC_RTC
RTC_INT_L
32KOUT_RTC2SOC
32KOUT_RTC2WIFI
32KOUT_Pcie
PMIC_EXT_EN_OUT
PWRON_L
PMIC_PWR_CTRL2
VCC_2V0_PLDO_S3
VCC5V0_SYS_S5
U2400
VIN
LX
GND
EN
FB/OUT
C2400 10uF X5R 10V C0603
C2408 NC/100nF X5R 10V C0402
R2405 100K R0402
PMIC_EXT_EN_OUT
L2400 1.0uH 3.22A 0.065ohm IND_252010
2.094V
C2403 100pF C0G 50V C0402
R2404 249K 1% R0402
R2408 100K 1% R0402
FB=0.6V
C2404 22uF X5R 6.3V C0603
C2405 100nF X5R 6.3V C0402
VCC_2V0_PLDO_S3
VCC_1V1_NLDO_S3
Option
VCC_2V0_PLDO_S3
R2400 NC/0R R0603
VCC_1V1_NLDO_S3_F
VCC5V0_SYS_S5
U2401
C2401 4.7uF X5R 10V C0603
C2409 NC/100nF TMI3112H /TCS4203 SOT_23_5
R2406 10K R0402
PMIC_EXT_EN_OUT
L2401 1.0uH 3.22A 0.065ohm IND_252010
FB=0.6V
C2402 100pF C0G 50V C0402
R2407 120K 1% R0402
R2403 100K 1% R0402
C2406 22uF X5R 6.3V C0603
C2407 100nF X5R 6.3V C0402
R2402 0R R0603
C2424 22uF X5R 6.3V C0805
VCC_1V8_S0
VCC_1V8_S3
Note:
1.8V Load Switch!
U2402
IN
VOUT
ON
GND
A2
A1
B2
B1
VCCA_1V8_S0
R2411 10K R0402
VCC_3V3_S0
R2416 NC/100K R0402
C2410 10uF X5R 6.3V C0603
R2413 100K R0402
CW3301 /TCS9719
WLCSP4_0R80x0R80x0R50
If the current is greater than 1.5A, multiple load switches need to be used for design
C2411 10uF X5R 6.3V C0603
Note:
Need quick output discharge
VCC_3V3_S3
VCC_3V3_S0
U2403
IN
VOUT
GND
EN
OCB
C2412 10uF X5R 6.3V C0603
R2412 470K R0402
C6740 100pF X5R 6.3V C0402
SGM2590D /TCS9163
SOT_23_5
Default:SGM2590D
Ilim=6612/RILIM*0.982(A)
Please design Ilim based on actual load
R2415 2.2K R0402
C2413 10uF X5R 6.3V C0603
PMIC_PWR_CTRL2
Q2405 2SK3018 SOT_323
VCC_3V3_S0
Note:
Need quick output discharge
RTC
VCC5V0_SYS_S5
2.5V<VIN<5.5V
U2404
IN
OUT
GND
EN
BP
Def:3.3V
VCC3V3_RTC_S5
C2414 1uF X5R 10V C0402
R2418 100K R0402
EN VIH=1.5V
C2416 NC/100nF X5R 10V C0402
TMI6050-33 /ETA5055V330DS2F SOT_23_5
C2417 NC/100nF X5R 6.3V C0402
C2415 4.7uF X5R 6.3V C0402
C2420 12pF C0G 50V C0402
Y2400 32.768KHz CRY2_6R90X1R40X1R30
C2422 NC/12pF C0G 50V C0402
RTC_INT_L
R2437 0R R0402
RTCINT_L
U2405
OSCI
OSCO
INT
VSS
VDD
CLKOUT
SCL
SDA
TCS8563 /IT8563UE
TSSOP8_3R10X3R10X1R10
VCC_RTC
32KOUT_RTC
I2C2_SCL_M0_CC_RTC
I2C2_SDA_M0_CC_RTC
C2421 100nF X5R 10V C0402
D2400 BAT54C SOT_23
VCC3V3_RTC_S5
J2400
CR1220-3V
BAT_CR1220
R2424 0R R0402 32KOUT_RTC2SOC
Default for SOC
R2425 0R R0402 32KOUT_RTC2WIFI
For WIFI
R6748 0R R0402 32KOUT_Pcie
VCC_1V8_S3
R2423 10K R0402
32KOUT_RTC
Audio Power
Note:
The voltage of VCCIO_CODEC is consistent with the voltage of VCCIO2
VCC_3V3_S0
VCCIO_CODEC
R2420 0R R0603
C2419 10uF X5R 6.3V C0603
CODEC
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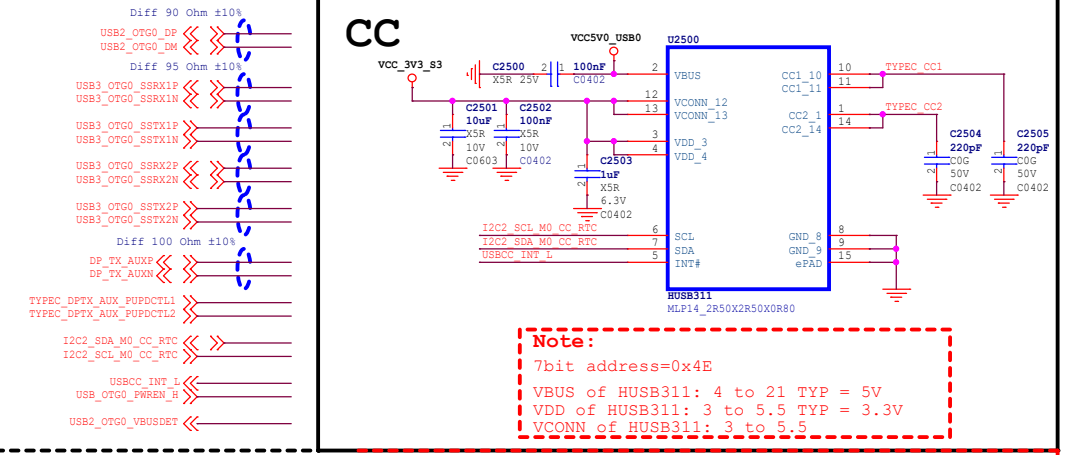
Rockchip Electronics Co., Ltd
Project: RK3576_AIOT_REF_SCH
File: 24.Power-Ext Discrete/RTC IC
Date: Monday, April 28, 2025
Rev: V1.0
Designed by: Wesley Huang
Reviewed by:
Sheet: 23 of 63

CC



Note:

7bit address=0x4E

VBUS of HUSB311: 4 to 21 TYP = 5V
VDD of HUSB311: 3 to 5.5 TYP = 3.3V
VCONN of HUSB311: 3 to 5.5

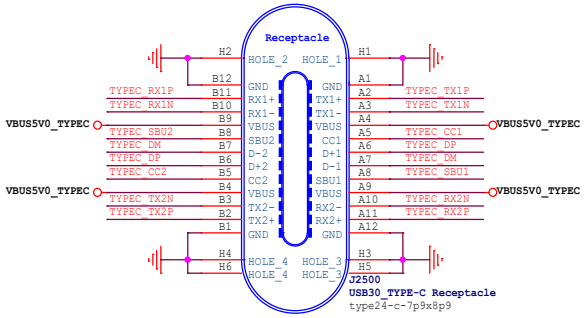
Note:

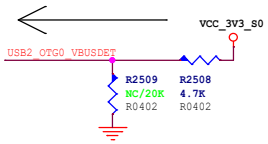
Different models of CC chips may require different driver software.

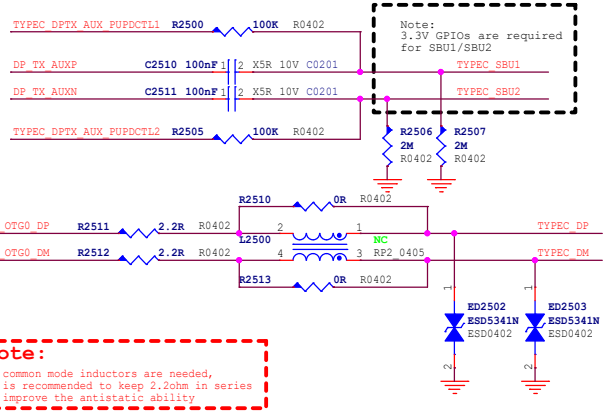
	AW35615(Default)	HUSB311(Option)
7bit address	0x22	0x4E
VBUS	4V~21V,TYP=5V	4V~21V,TYP=5V
VDD	2.7V~5.5V,TYP=3.3V	3V~5.5V,TYP=3.3V
VCONN	2.7V~5.5V	3V~5.5V

TYPEC

With Displayport Alt Mode
This is also the firmware download interface

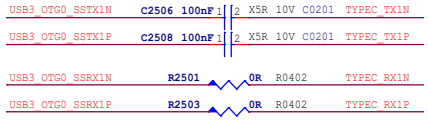


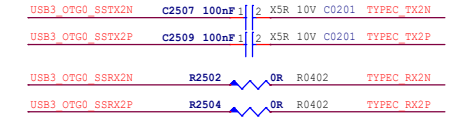




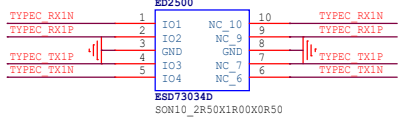
Note:

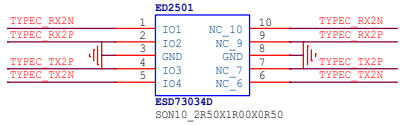
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability

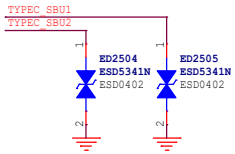


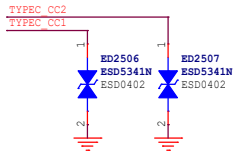


Cj<=0.2pF

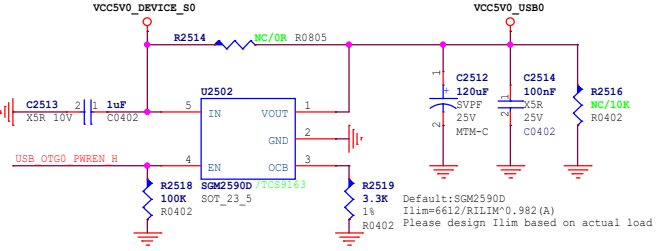


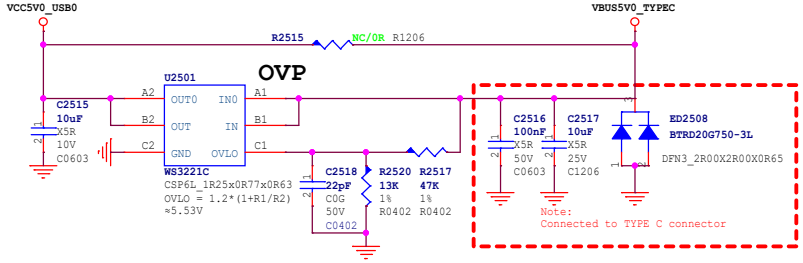






USB POWER





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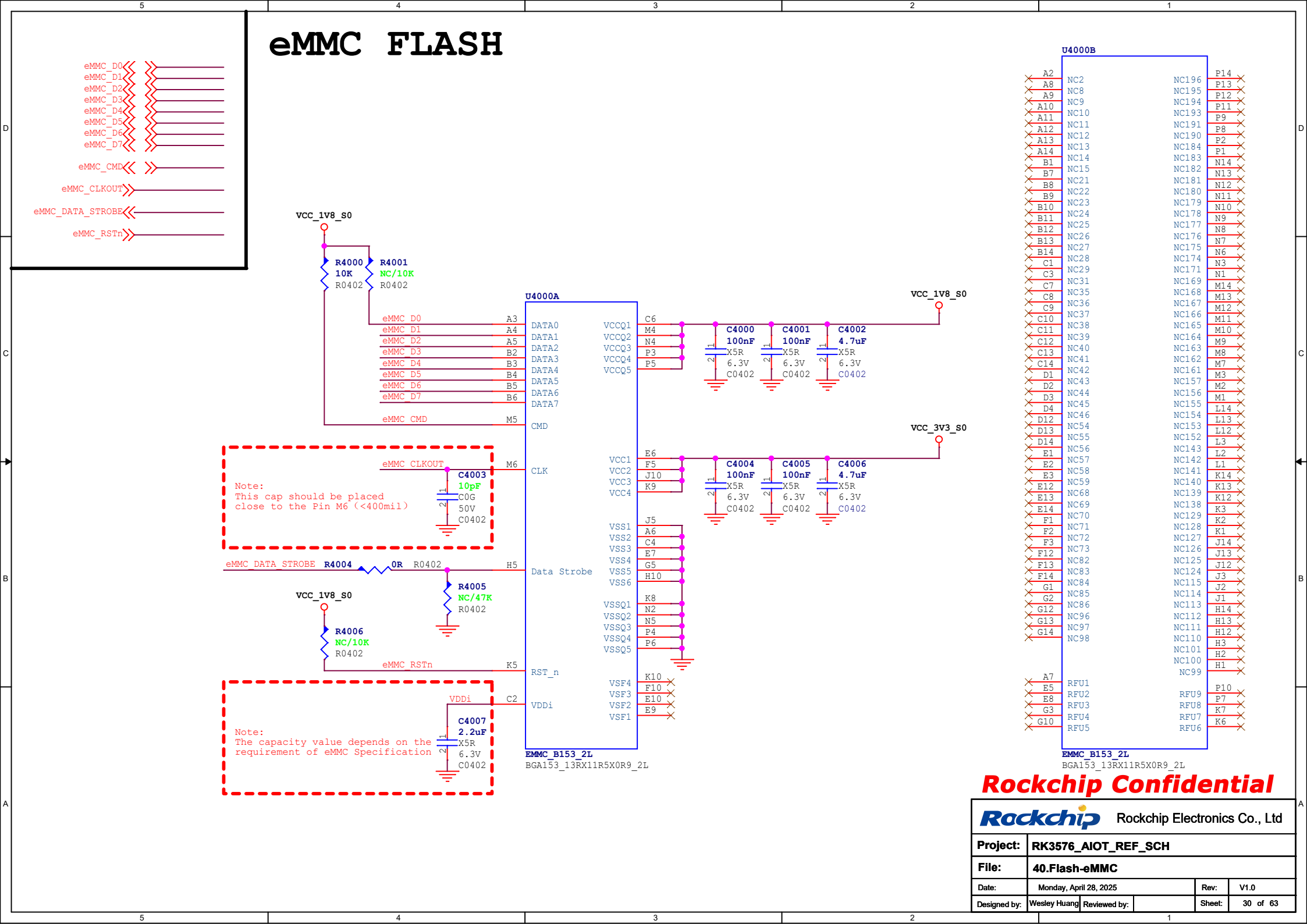
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	25.USB0-Type C Port With DP Alt				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	24 of 63

eMMC FLASH



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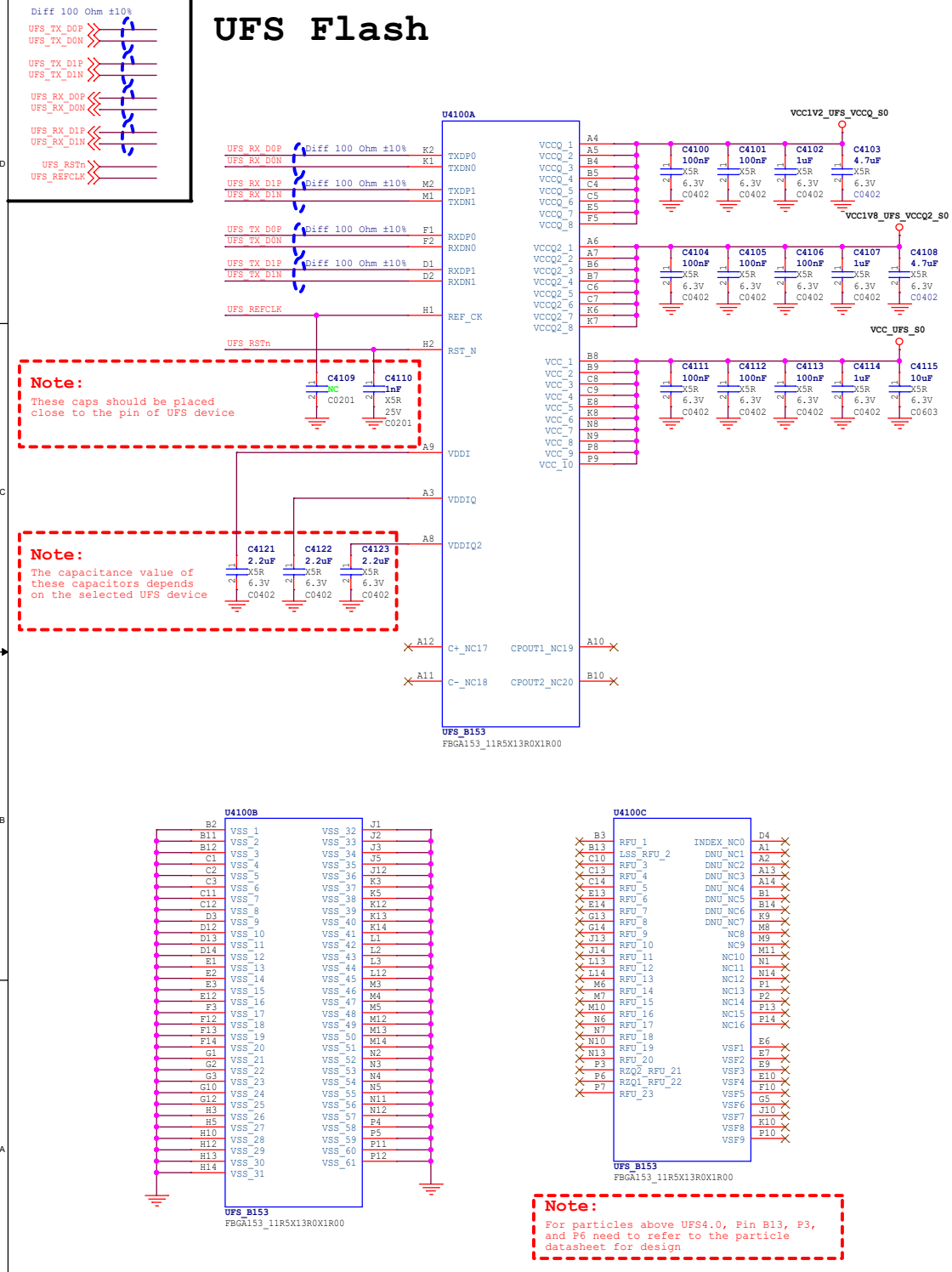
Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	40.Flash-eMMC		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by: Wesley Huang	Reviewed by:	Sheet:	30 of 63

UFS Flash



Note:
These caps should be placed close to the pin of UFS device

Note:
The capacitance value of these capacitors depends on the selected UFS device

Note:
For particles above UFS4.0, Pin B13, P3, and P6 need to refer to the particle datasheet for design

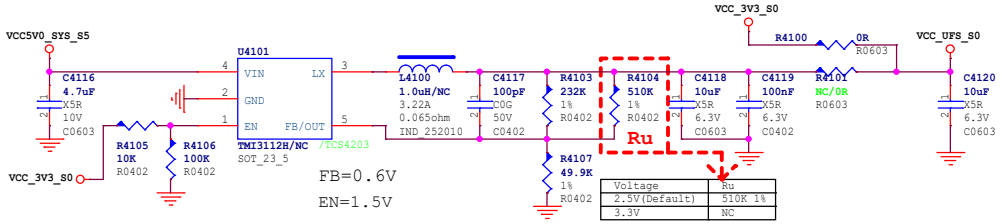
UFS POWER

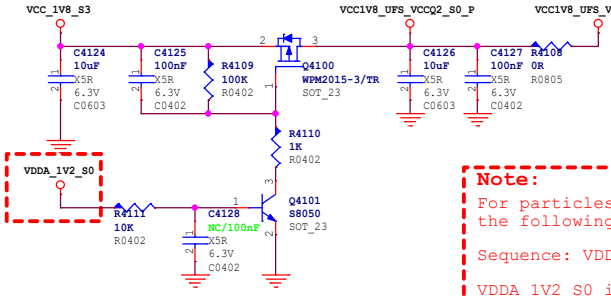
Supported Particles	VCCQ	VCCQ2	VCC	
UFS2.0	1.2V	1.8V	3.3V	Default UFS device: UFS2.2
UFS2.1	No Connect	1.8V	3.3V	
UFS2.2	No Connect	1.8V	3.3V	
UFS3.0	1.2V	No Connect	2.5V/3.3V	
UFS3.1	1.2V	No Connect	2.5V/3.3V	

Do not support UFS4.0 Device!

Sequence:VCCQ2->VCCQ, VCC is independent

Note:
The power ball that is not used at the particle must be kept floating.

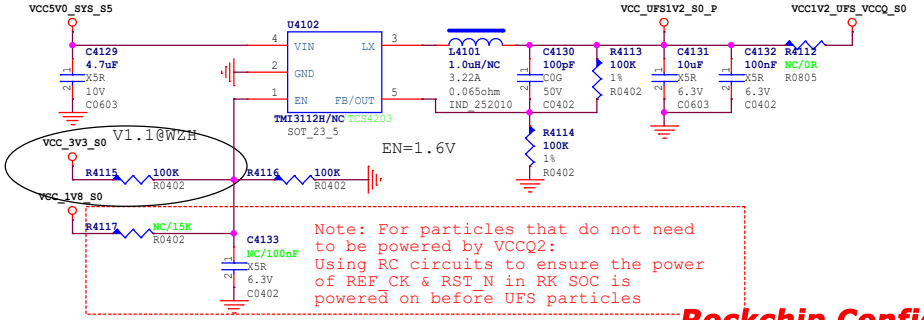




Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:

Sequence: VDDA_1V2_S0->VCCQ2->VCCQ

VDDA_1V2_S0 is the power of REF_CK & RST_N in RK SOC, which needs to be powered on before UFS particles



Note: For particles that do not need to be powered by VCCQ2:
Using RC circuits to ensure the power of REF_CK & RST_N in RK SOC is powered on before UFS particles

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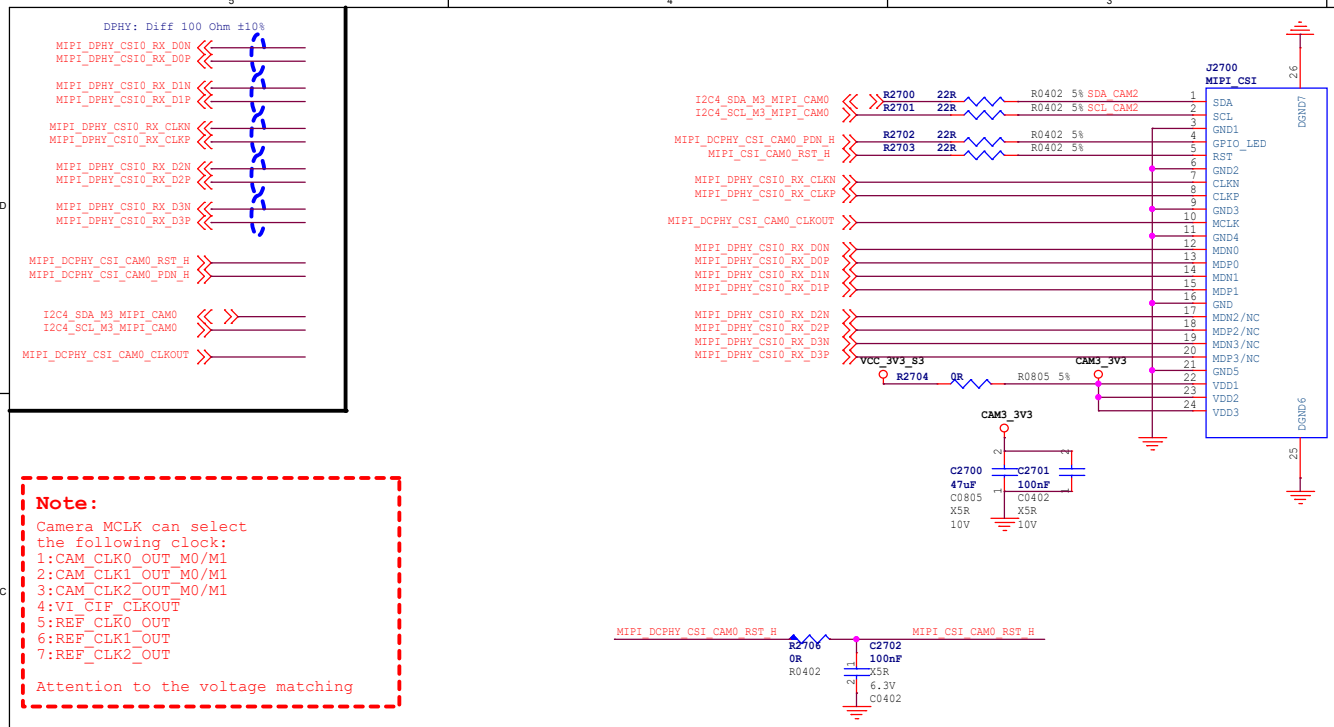
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	41.Flash-UFS		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet: 31 of 63



Note:

Camera MCLK can select the following clock:

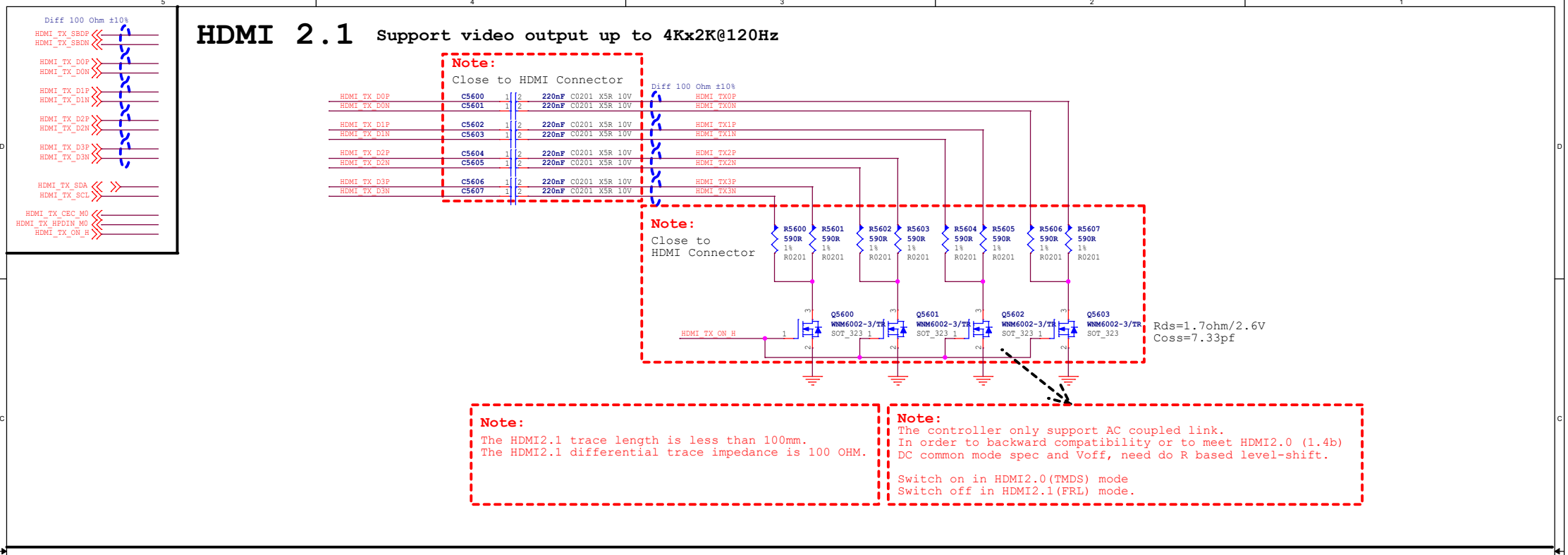
1:CAM_CLK0_OUT_M0/M1
2:CAM_CLK1_OUT_M0/M1
3:CAM_CLK2_OUT_M0/M1
4:VI_CIF_CLKOUT
5:REF_CLK0_OUT
6:REF_CLK1_OUT
7:REF_CLK2_OUT

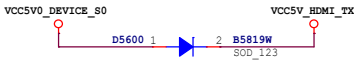
Attention to the voltage matching

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	27.VI-CAM MIPI DPHY CSI0 RX				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	34 of 63

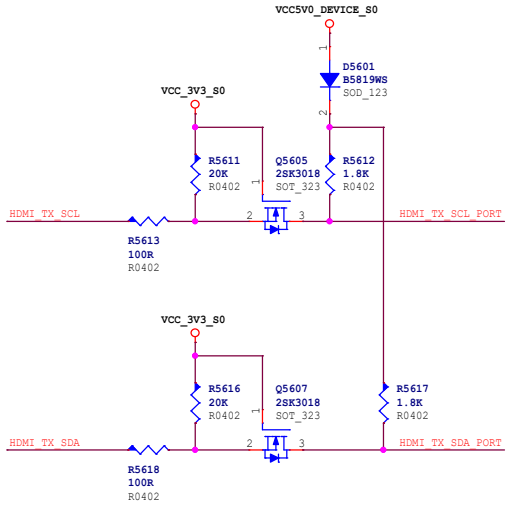
HDMI 2.1

Support video output up to 4Kx2K@120Hz



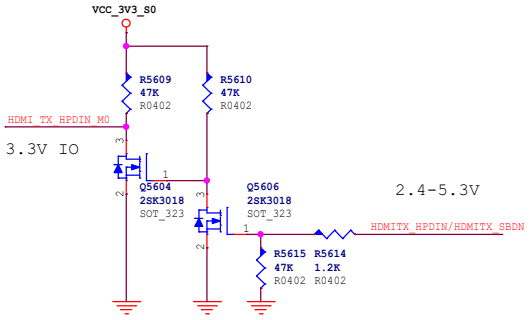


HDMI TX DDC

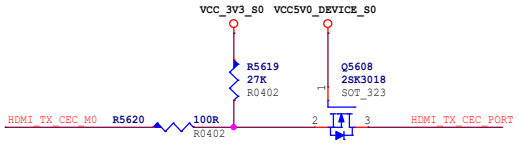


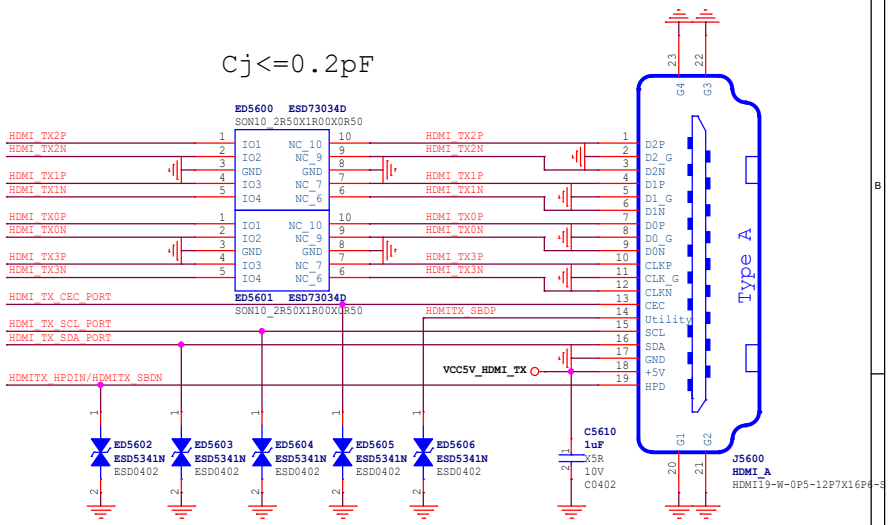
HDMI TX ARC

HDMI TX HPD



HDMI TX CEC





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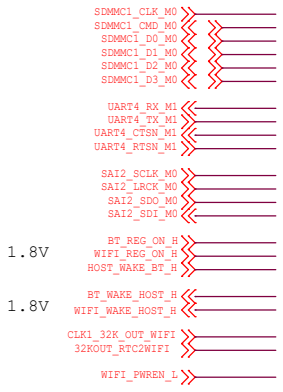
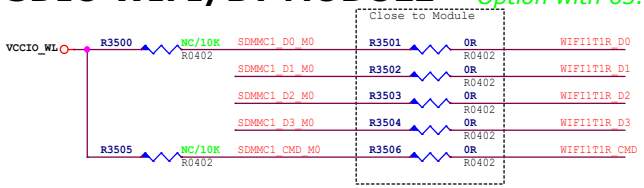
Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	56.VO-HDMI TX				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	41 of 63

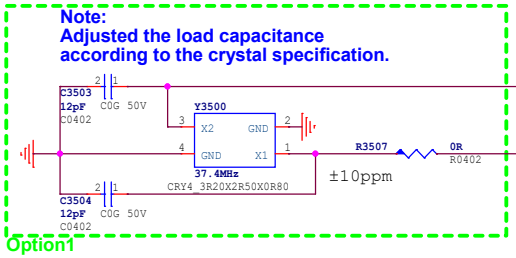
SDIO WIFI/BT MODULE

Option with 63.WIFI6/BT-SDIO+UART_2T2R

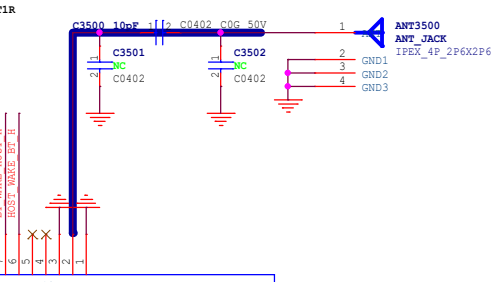




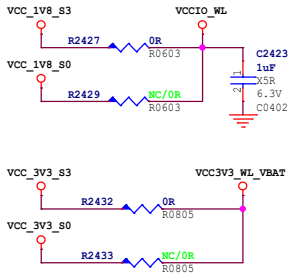
Note:
The maximum peak current is 600mA
Close to WIFI module

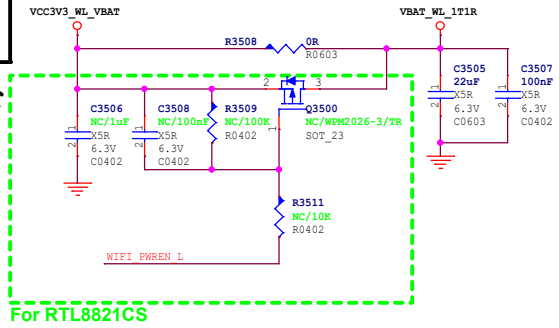


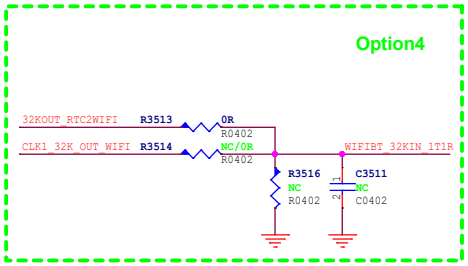
50 Ohm RF trace

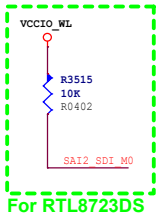


WIFI/BT Power

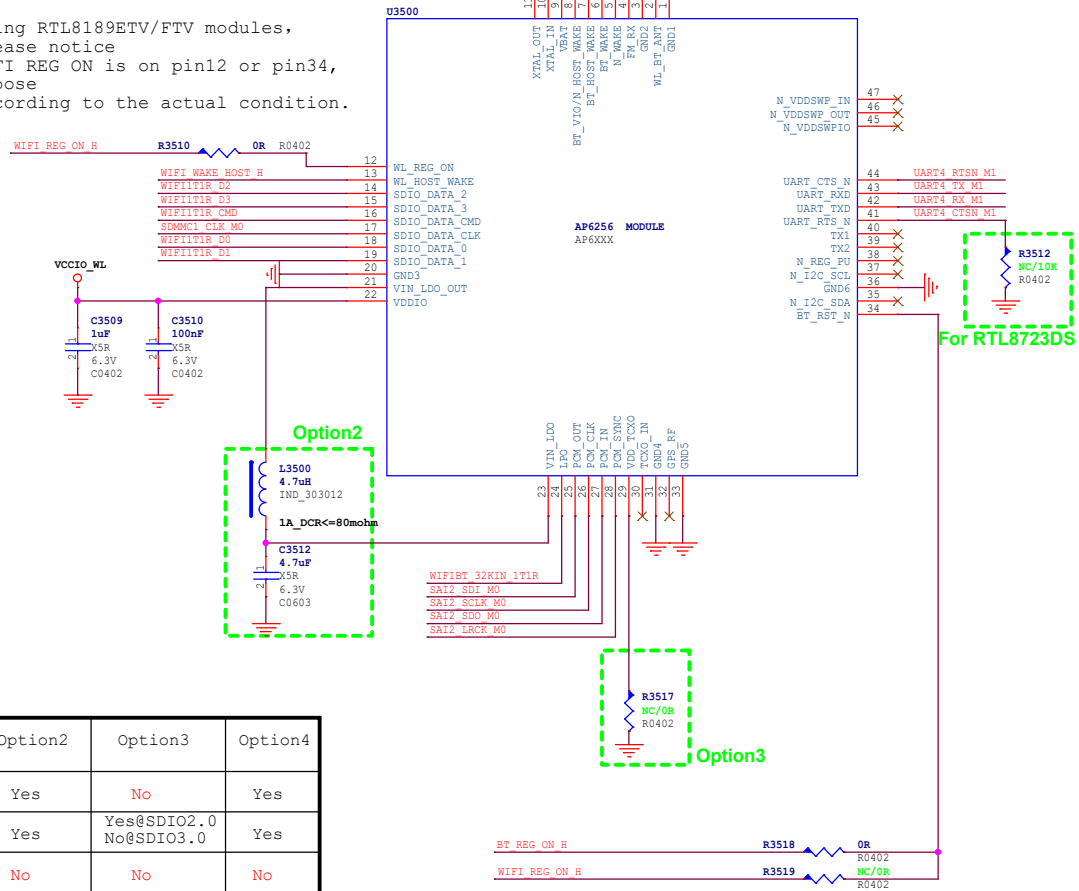








Using RTL8189ETV/FTV modules,
please notice
WIFI REG ON is on pin12 or pin34,
choose
according to the actual condition.



Using RTL8189ETV/FTV modules, please notice
WIFI REG ON is on pin12 or pin34, choose
according to the actual condition.

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

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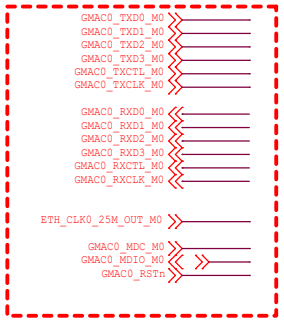
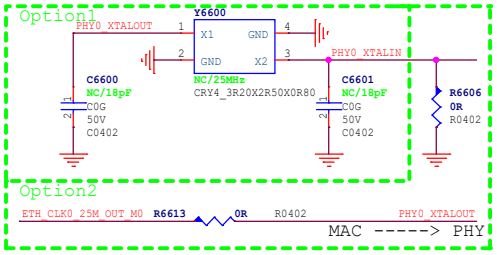
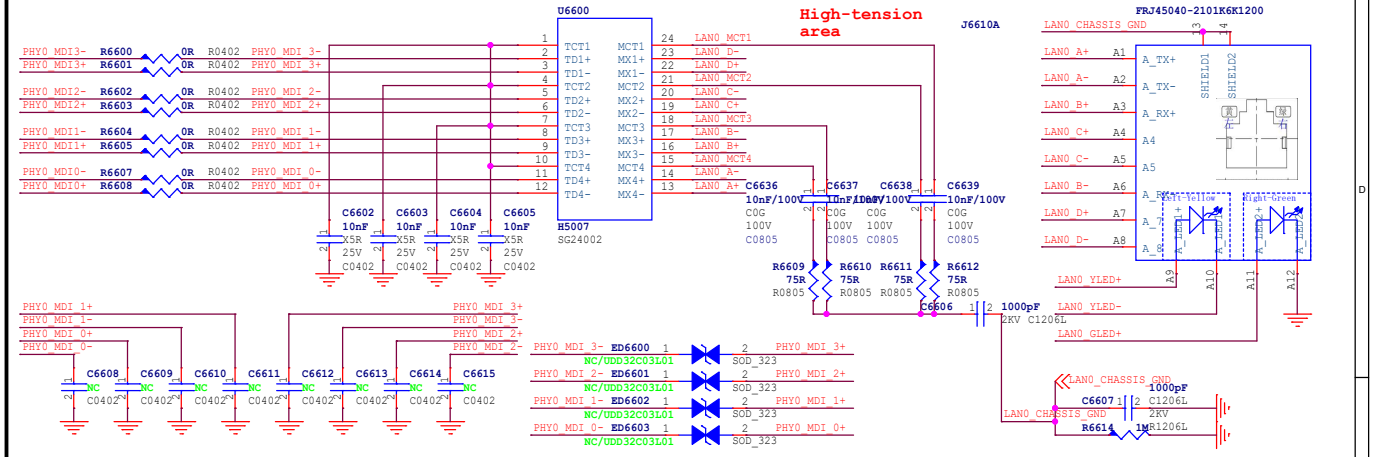
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	35.WIFI/BT-SDIO+UART_1T1R(Opt)		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet: 43 of 63

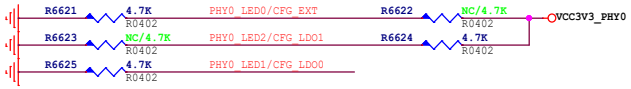
RGMII0_M0







RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY0_LED2
External 3.3V	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V (default)	1'b0	2'b10	String 510R to VCC3V3_PHY

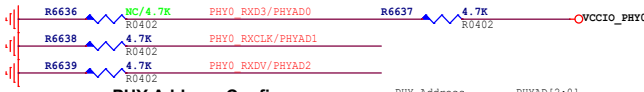


VCC_PHY0_IO Voltage Config

Pull-up to disable PLL @ ALDPS mode(Low power mode)

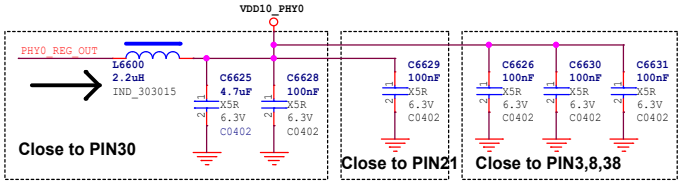
Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

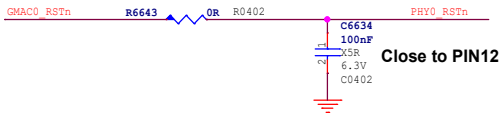


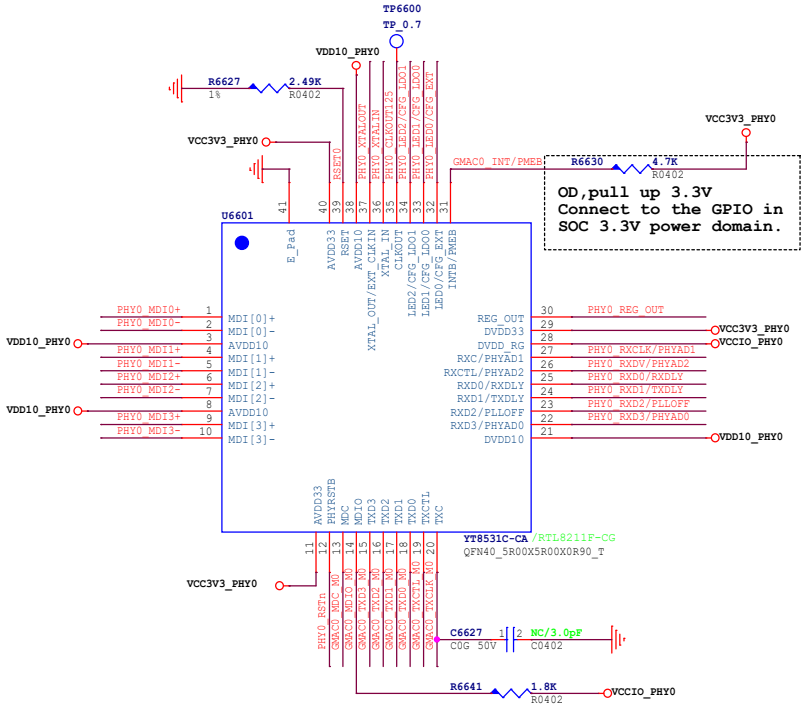
PHY Address Config

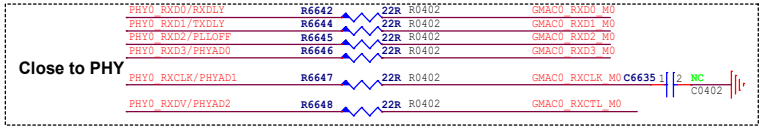
PHY Address	PHYAD[2:0]
1 (default)	3'b001



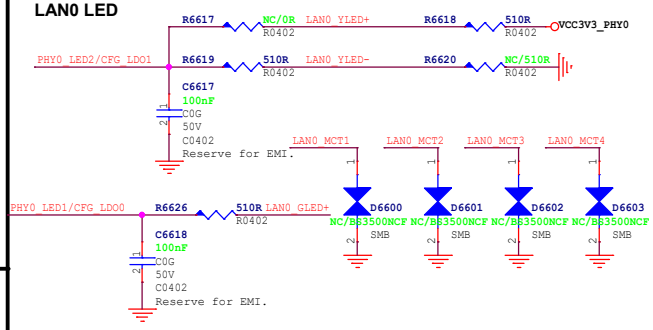
PHYRSTB is 3.3V IO

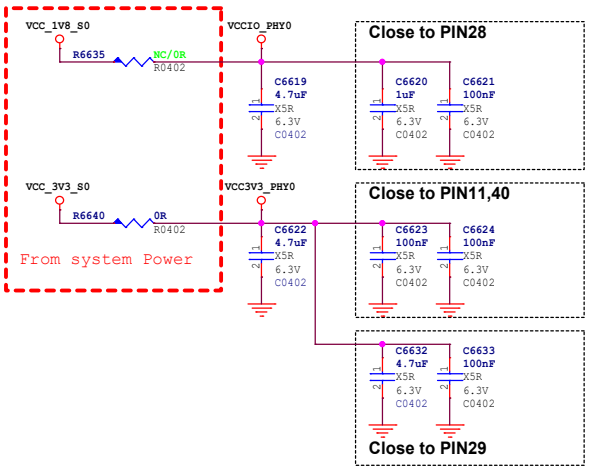






LAN0 LED

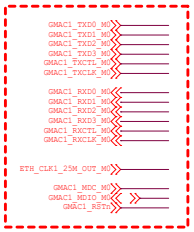


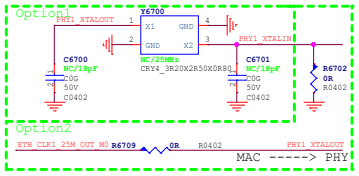


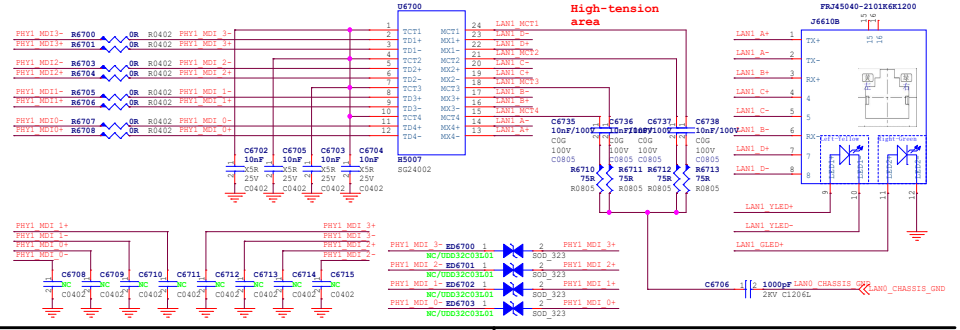
Rockchip Confidential

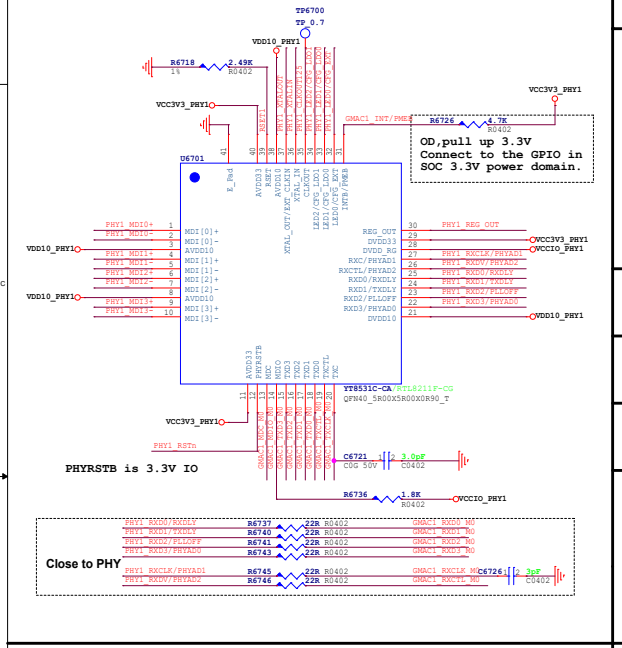
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	66.Ethernet-GEPHY_RGMII0		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet: 48 of 63

RGMII1_M0



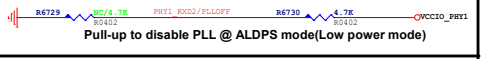






RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY1_LED2
External 3.3V (default)	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V	1'b0	2'b10	String 510R to VCC3V3_PHY

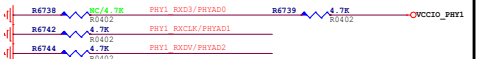
VCC_PHY0_IO Voltage Config



Pull-up to disable PLL @ ALDPS mode(Low power mode)

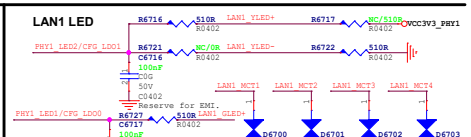
Pull-up for additional 2ns delay to RXC for data latching

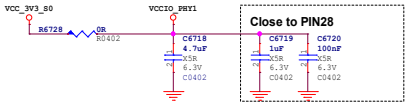
Pull-up for additional 2ns delay to TXC for data latching

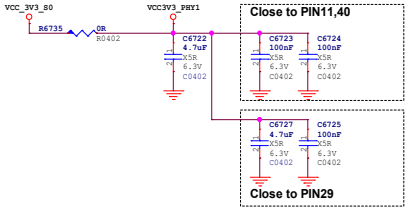


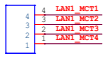
PHY Address	PHYAD[2:0]
1 (default)	3'b001

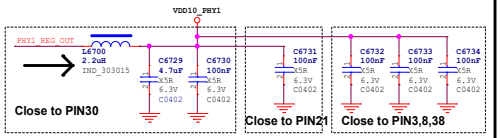
PHY Address Config





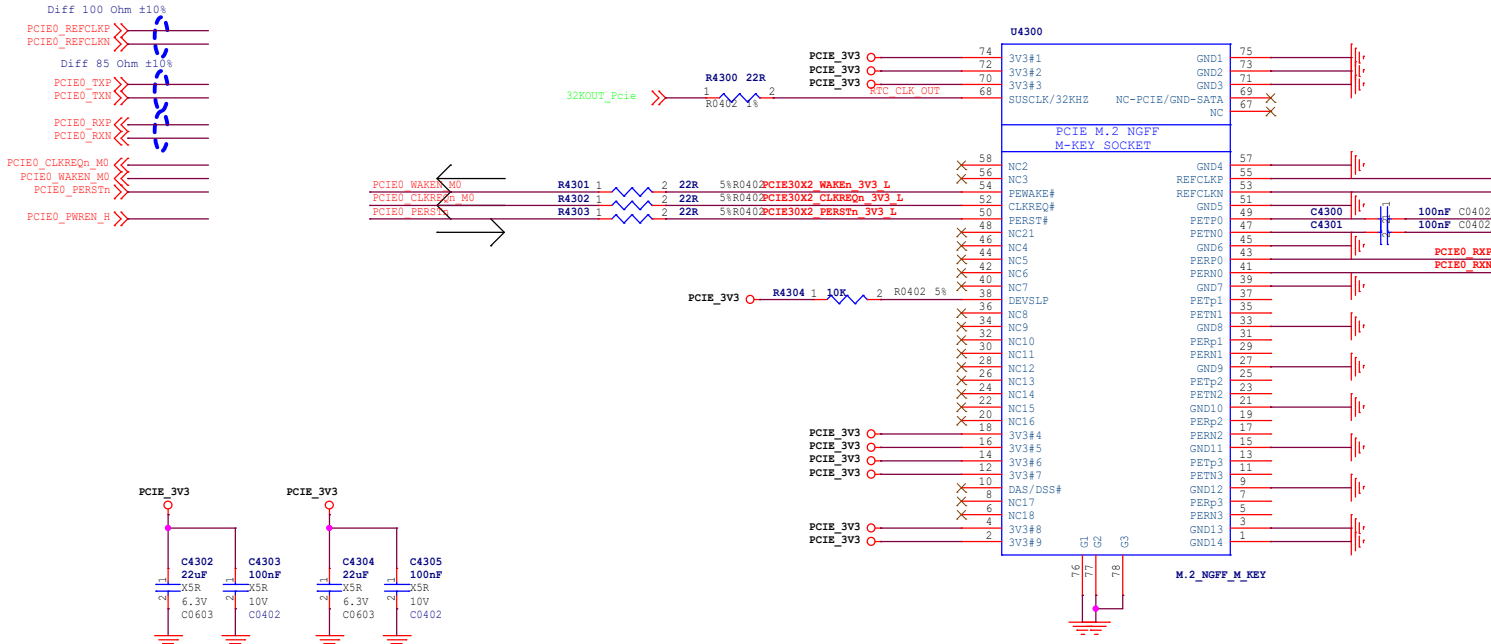


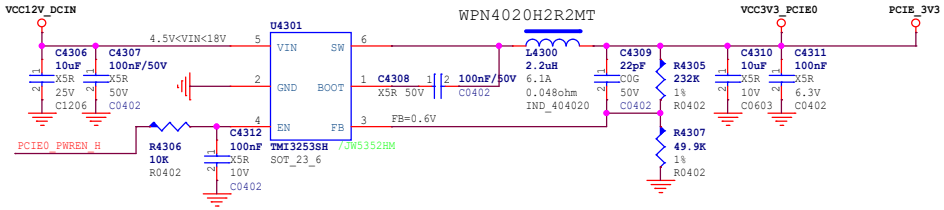




Rockchip Confidential

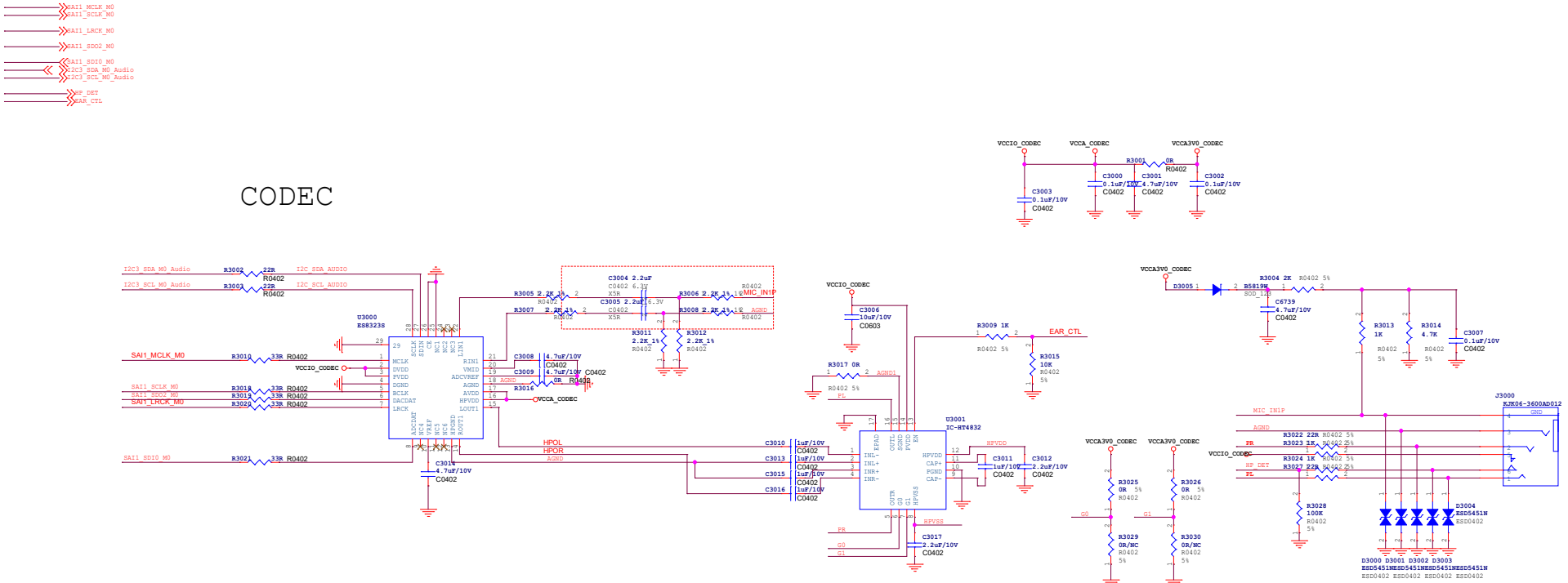
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3576_AIOT_REF_SCH		
File:	67.Ethernet-GEPHY_RGMII1		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by: Wesley Huang	Reviewed by:	Sheet:	49 of 63





ShenZhen HugSun Technology Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	43.M2 Pcie		
Date:	Friday, October 17, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	51 of 99

CODEC



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3576_AIOT_REF_SCH
File:	30.Audio-S
Date:	Monday, April 28, 2025
Rev:	V1.0
Designed by:	Wesley Huang
Reviewed by:	
Sheet:	53 of 63

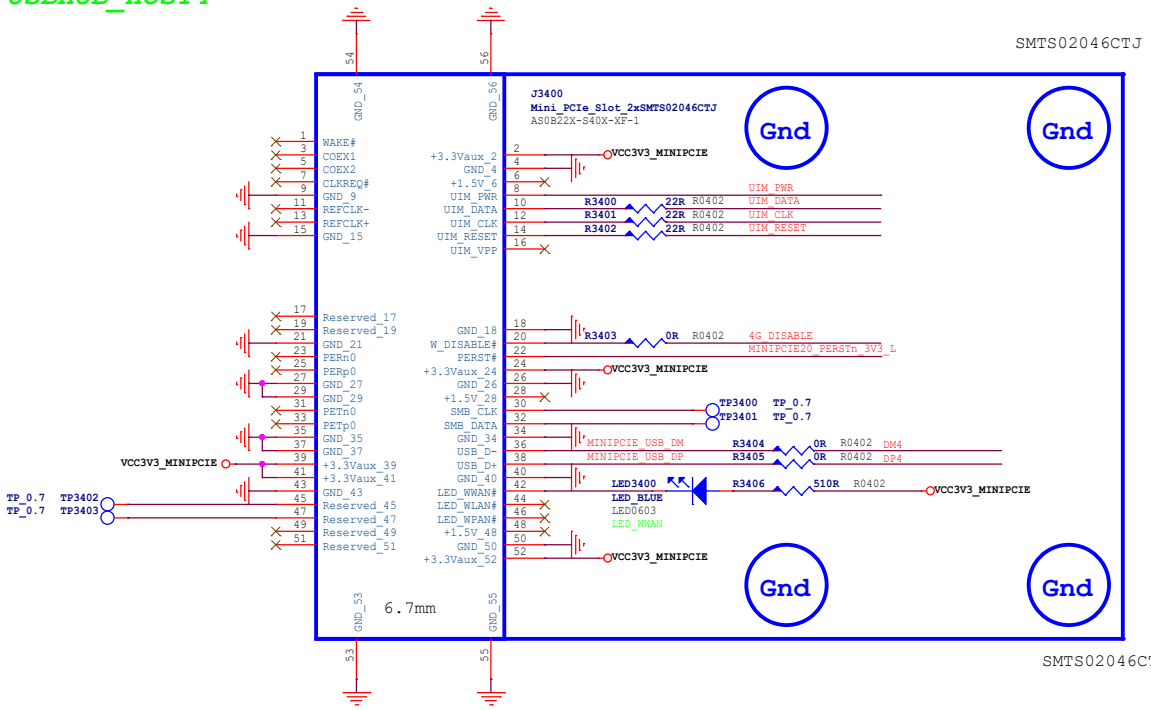
MiniPCIe Slot with 4G Function

(12V DC Power Supply is required)

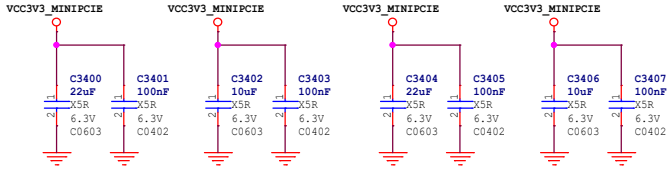
Option with 81.PCIe-PCIe Slot_36P and USBHUB_HOST4

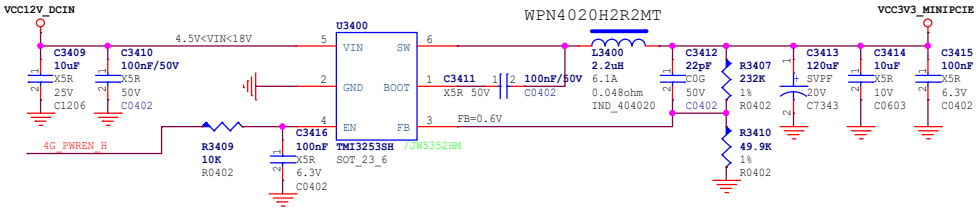
DP4
DM4
4G_PWREN_H
4G_DISABLE
4G_RST
SIM_DET

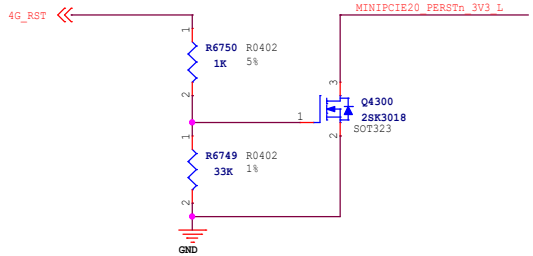
SMTS02046CTJ



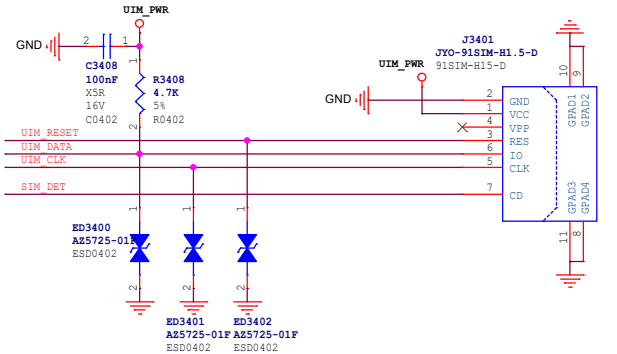
SMTS02046CTJ







SIM CARD

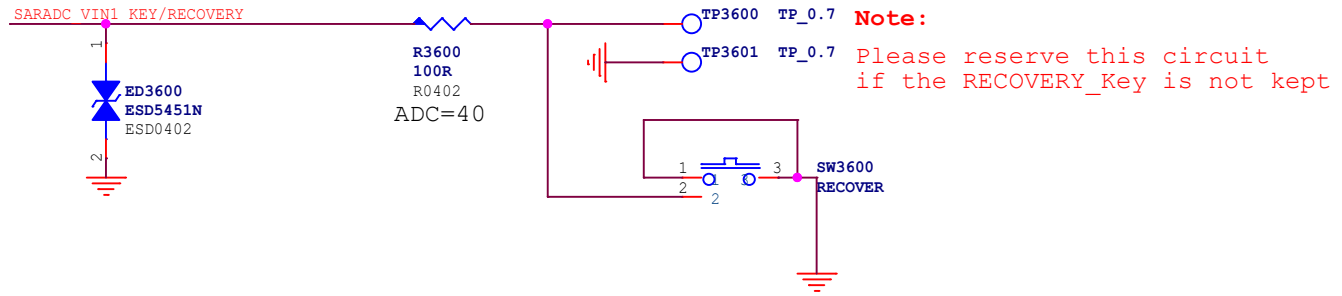


Rockchip Confidential

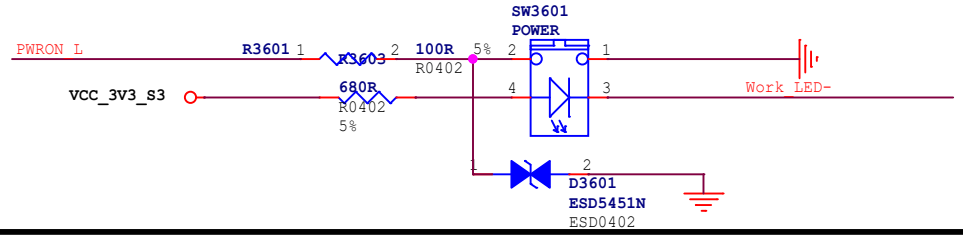
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH				
File:	34.MiniPCIe Slot_with 4G(Opt)				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	55 of 63

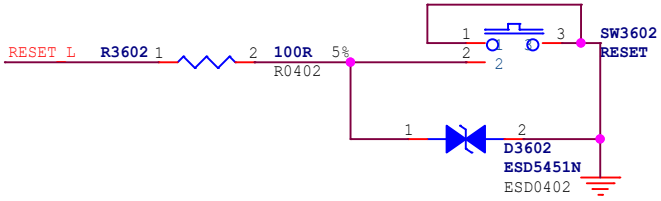
SARADC_VIN1_KEY/RECOVERY
RESET_L
PWRON_L
SARADC_VIN0_BOOT
Work_LED-

KEY

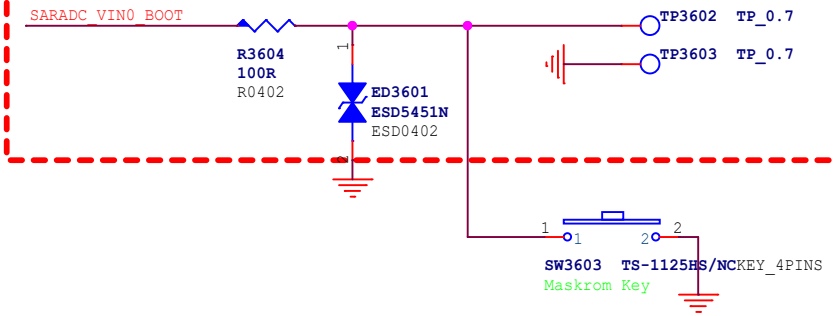


Note:
Please reserve this circuit
if the RECOVERY_Key is not kept





MASKROM Key



Note:
Please reserve this circuit
if the MASKROM_Key is not kept

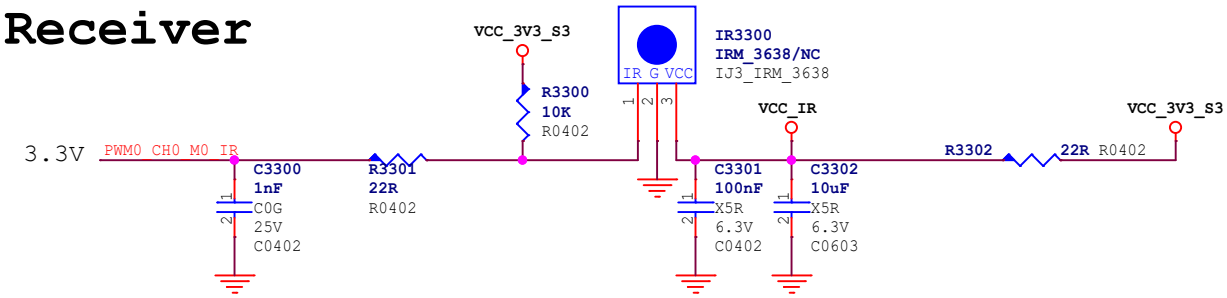
Note:
If BOOT_SARADC_IN0=0V after power-on reset,
then system will enter into MASKROM mode.

Rockchip Confidential

Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH			
File:	36.Key-PowerON/Reset/V+/V-/etc			
Date:	Monday, April 28, 2025		Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet:	57 of 63

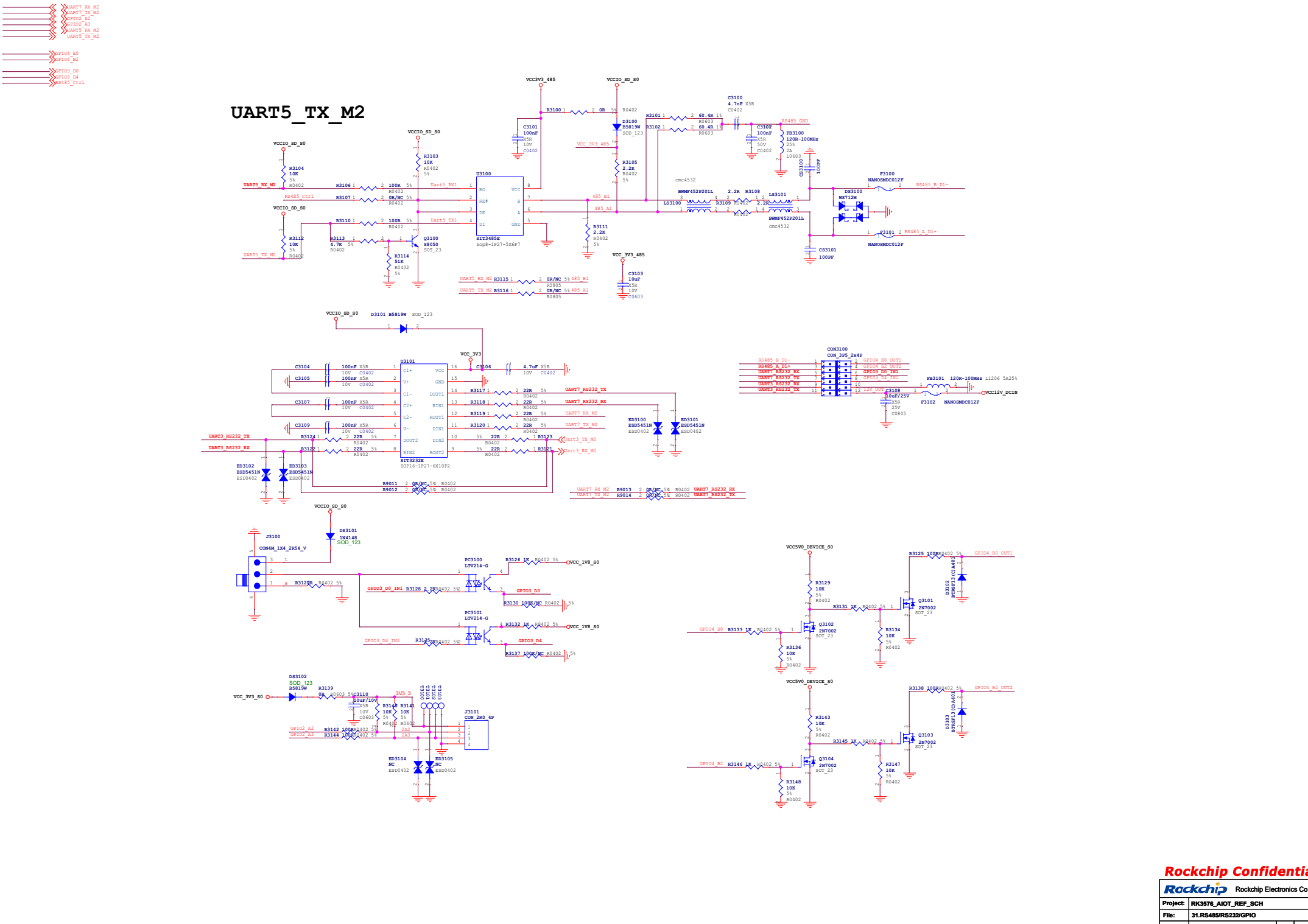
PWM0_CH0_M0_IR

IR Receiver

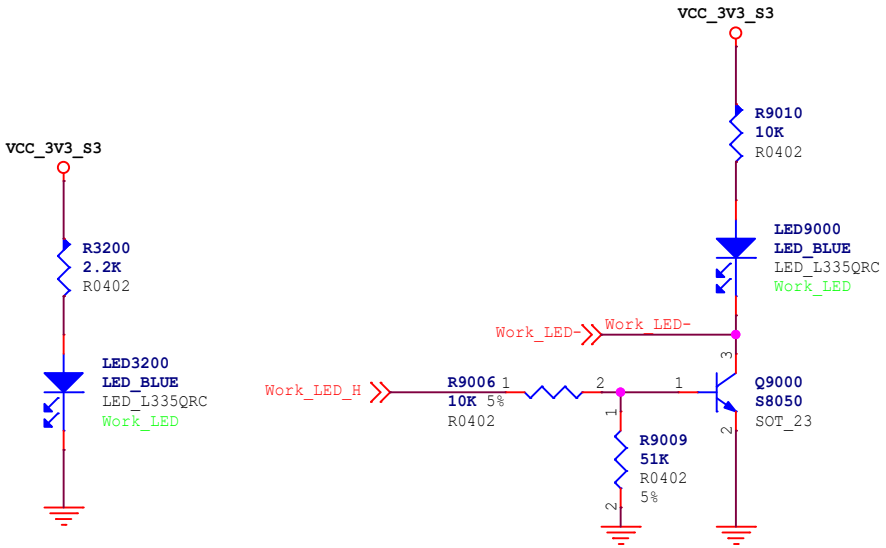


Rockchip Confidential

Rockchip Electronics Co., Ltd				
Project:	RK3576_AIOT_REF_SCH			
File:	33.Sensors/IR Receiver			
Date:	Monday, April 28, 2025		Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:	Sheet:	58 of 63


UART5_TX_M2
UART7_RX_M2
UART7_TX_M2
GPIO2_A2
GPIO2_A3
UART5_RX_M2
UART5_TX_M2
GPIO4_B0
GPIO4_B2
GPIO3_D0
GPIO3_D4
RS485_Ctrl
VCC3V3_485
VCCIO_SD_S0
U3100
SIT3485E
U3101
SIT3232E
CON3100
J3100
J3101
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK3576_AIOT_REF_SCH
File: 31.RS485/RS232/GPIO
Date: Tuesday, April 29, 2025
Rev: V1.0
Designed by: Wesley Huang
Reviewed by:
Sheet: 59 of 63

Work_LED



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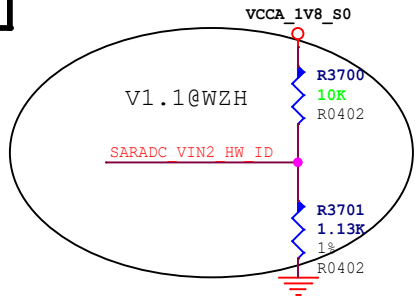
Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	32.LED		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by: Wesley Huang	Reviewed by:	Sheet:	60 of 63

SARADC_VIN2_HW_ID

HW_ID



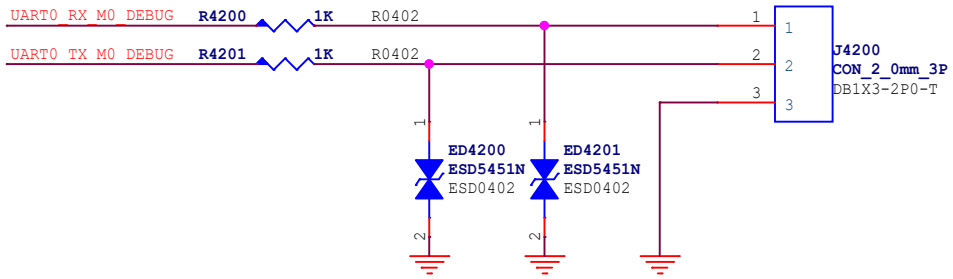
Config Table for SARADC_VIN2_HW_ID

Item	Rup	Rdown	ADC Value	VERSION
HW_ID1	NC	10K	0	RESERVE
HW_ID2	10K	1.13K	416	HW_ID1
HW_ID3	10K	2.49K	816	RESERVE
HW_ID4	10K	4.3K	1231	RESERVE
HW_ID5	10K	6.8K	1658	RESERVE
HW_ID6	10K	10K	2048	RESERVE
HW_ID7	10K	14.7K	2437	RESERVE
HW_ID8	10K	23.2K	2862	RESERVE
HW_ID9	10K	40.2K	3279	RESERVE
HW_ID10	10K	88.7K	3680	RESERVE
HW_ID11	10K	NC	4095	RESERVE

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	37.HW_ID				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	61 of 63

UART0_RX_M0_DEBUG
UART0_TX_M0_DEBUG

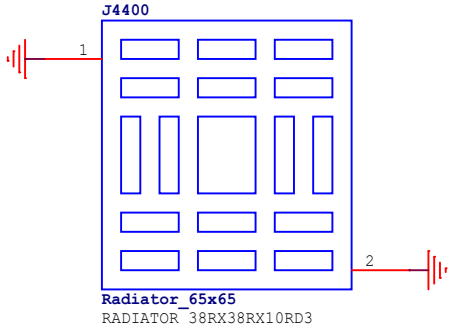
Debug UART_M0



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3576_AIOT_REF_SCH				
File:	42.Debug UART				
Date:	Monday, April 28, 2025			Rev:	V1.0
Designed by:	Wesley Huang	Reviewed by:		Sheet:	62 of 63

Heatsink

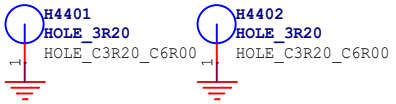


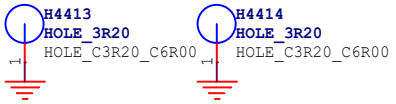
Mark

TOP Mark

BOTTOM Mark

Hole





Rockchip Electronics Co., Ltd			
Project:	RK3576_AIOT_REF_SCH		
File:	44.Mark/Hole/Heatsink		
Date:	Monday, April 28, 2025	Rev:	V1.0
Designed by:	Wesley Huang / Reviewed by:	Sheet:	63 of 63