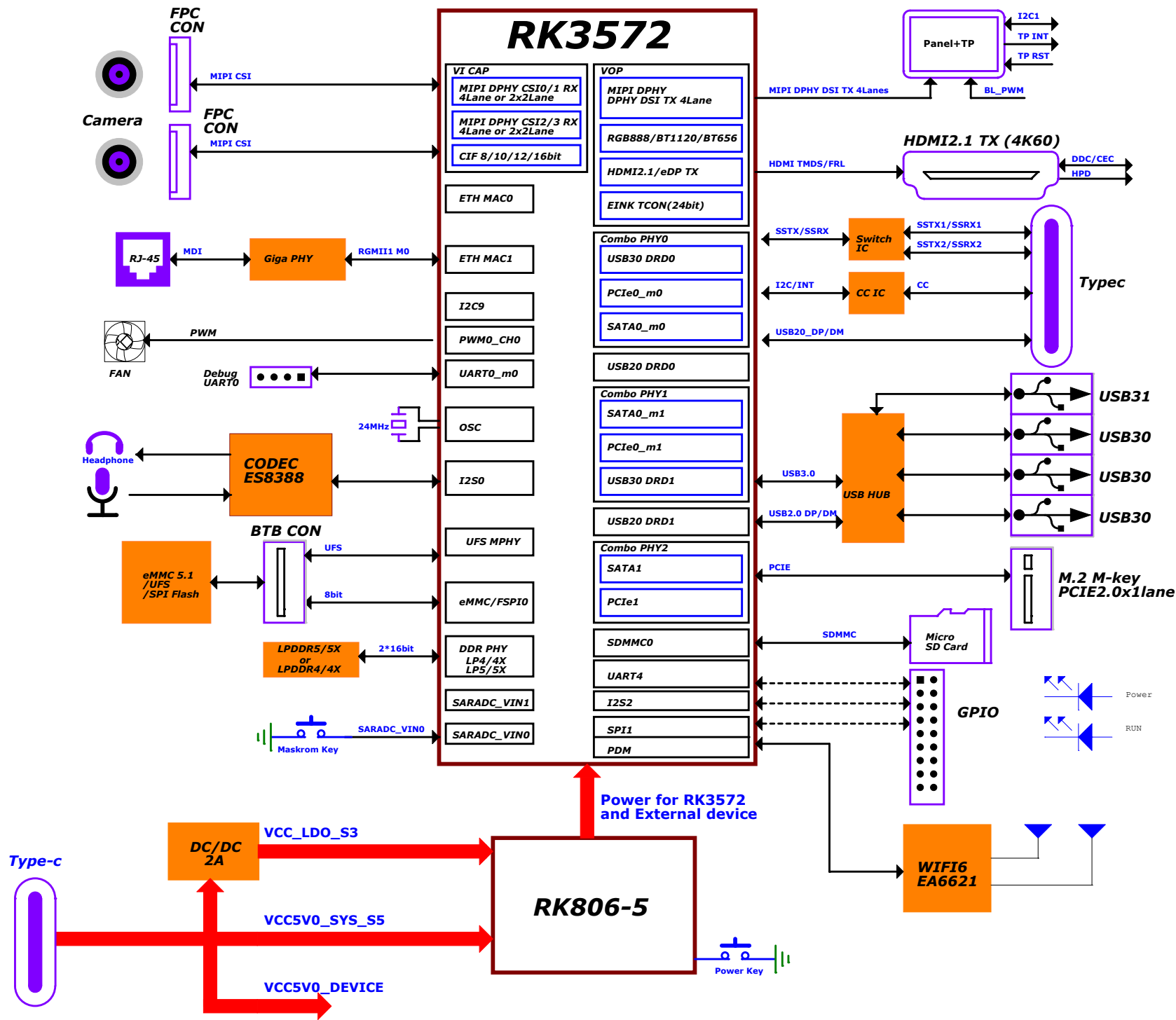
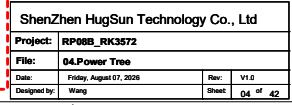


RK3572 Block Diagram



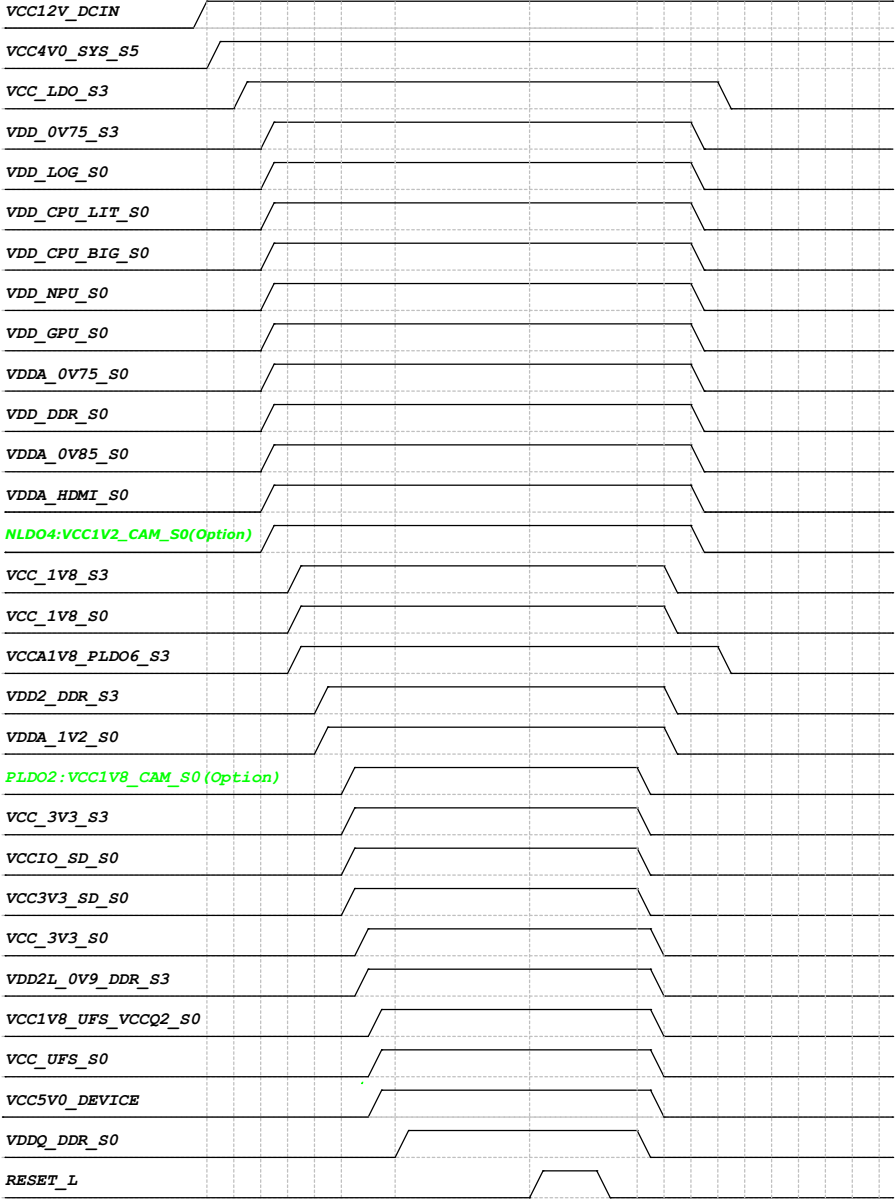
VCC12V_DCIN



Power Sequence

Power on Slot Power off Slot

0 1 2 3 4 5 7 12 1 2 3 4



Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Power Description

Power Supply	PMIC Channel	Supply Limit	Power Name	Power on Slot	Default Voltage	Default ON/OFF	Work Voltage	Power off Slot	NOTE
VCC4V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	Slot:3	
VCC4V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	Slot:3	
VCC4V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	Slot:3	
VCC4V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	Slot:1	
VCC4V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	Slot:3	
VCC4V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-4x/0.75V-LP4	Slot:1	
VCC4V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0	Slot:2	0.75V	ON	0.51V-LP5	Slot:3	
VCC4V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S0	Slot:3	1.8V	ON	1.8V	Slot:2	
VCC4V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x	Slot:2	
VCC4V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	1.05V-LP5	Slot:3	
VCC_LDO_S3	RK806_PLDO1	0.5A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	Slot:2	
	RK806_PLDO2	0.3A	VCC1V8_CAM_S0(Option)	Slot:5	1.8V	ON	1.8V	Slot:1	
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	Slot:2	
VCC4V0_SYS_S5	RK806_PLDO4	0.5A	VCC3V3_SD_S0	Slot:5	3.0V	ON	3.3V	Slot:1	
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	Slot:1	
VCC4V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	Slot:4	
VCC_LDO_S3	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	Slot:3	
	RK806_NLDO2	0.3A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	Slot:3	
	RK806_NLDO3	0.5A	VDDA_HDMI_S0	Slot:2	0.75V	ON	0.8375V	Slot:3	
VCC_LDO_S3	RK806_NLDO4	0.5A	VCC1V2_CAM_S0(Option)	Slot:2	0.85V	ON	1.2V	Slot:3	
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	Slot:3	
	RK806_RESETh								
VCC12V_DCIN	EXT BUCK	3A	VCC4V0_SYS_S5	Slot:0	5.0V	ON	5.0V		
VCC4V0_SYS_S5	EXT BUCK	2A	VCC_LDOIN_S3	Slot:1	2.1V	ON	2.0V	Slot:4	
VCC_3V3_S3	SWITCH		VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	Slot:1A	
VCC4V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	Slot:1A	
VCC4V0_SYS_S5	EXT BUCK	2A	VCC_UFS_S0	Slot:5B	2.5V/3.3V	ON	2.5V/3.3V	Slot:1A	
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE	Slot:5B	5.2V	ON	5.2V	Slot:1A	
VCC4V0_SYS_S5	EXT BUCK	2A	VCC_UFS_VDDQ2_S0	Slot:5B	1.2V/1.8V	ON	1.2V/1.8V	Slot:1A	

Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2G11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 2G10	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 2P2	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2B2	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2D2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2P5	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2C2	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2K11/2K12	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2L12	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2A10	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

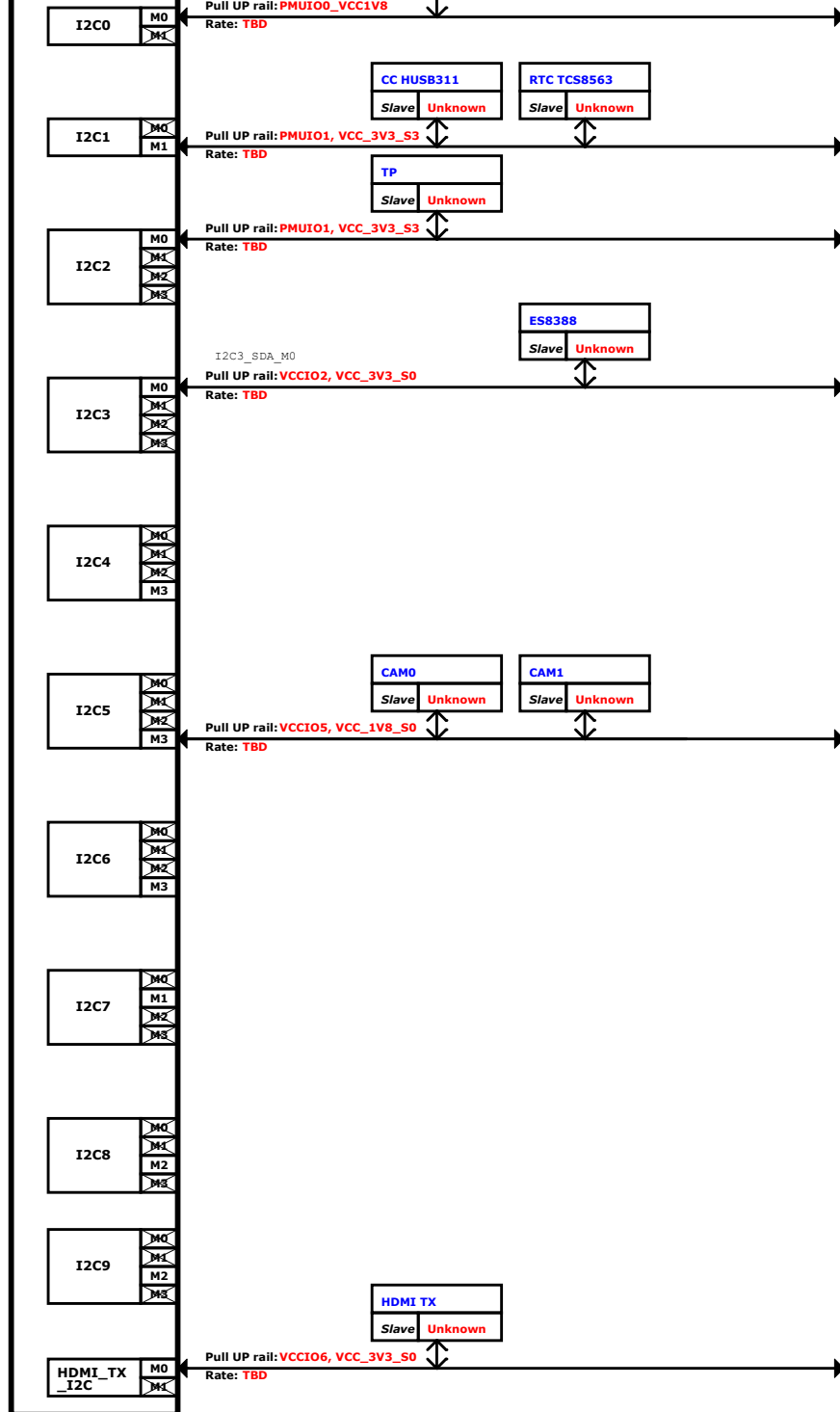
IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

ShenZhen HugSun Technology Co., Ltd

Project:	RP08B_RK3572		
File:	05.Power Sequence and Map		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	05 of 42

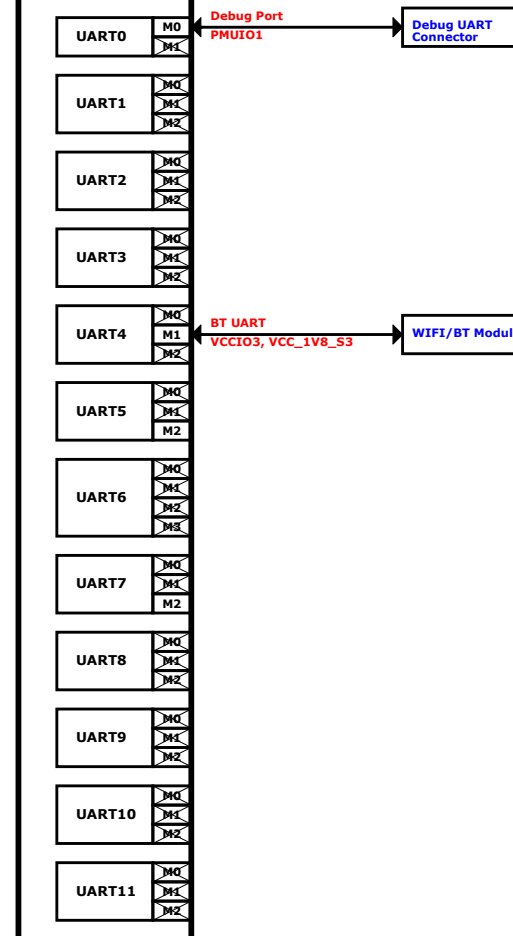
I2C MAP

RK3572



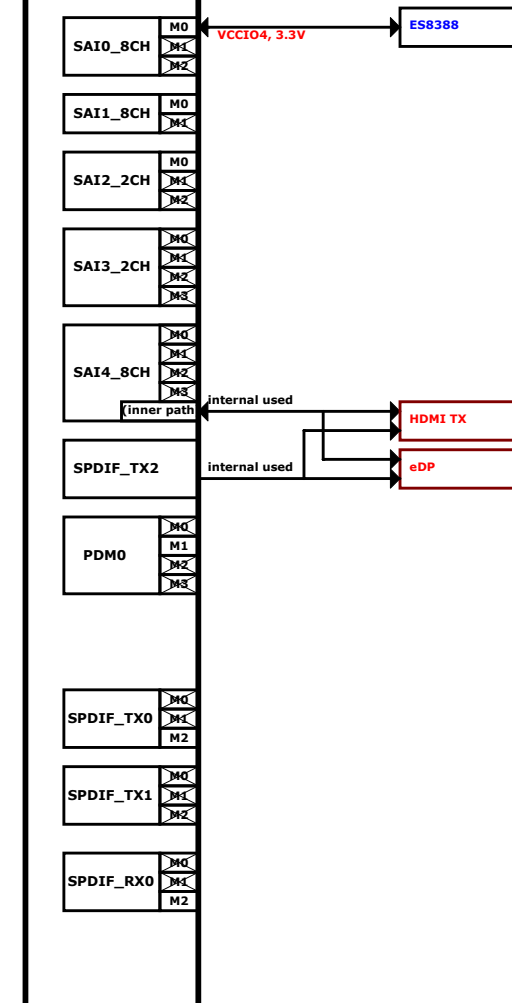
UART MAP

RK3572



Audio MAP

RK3572



Note:



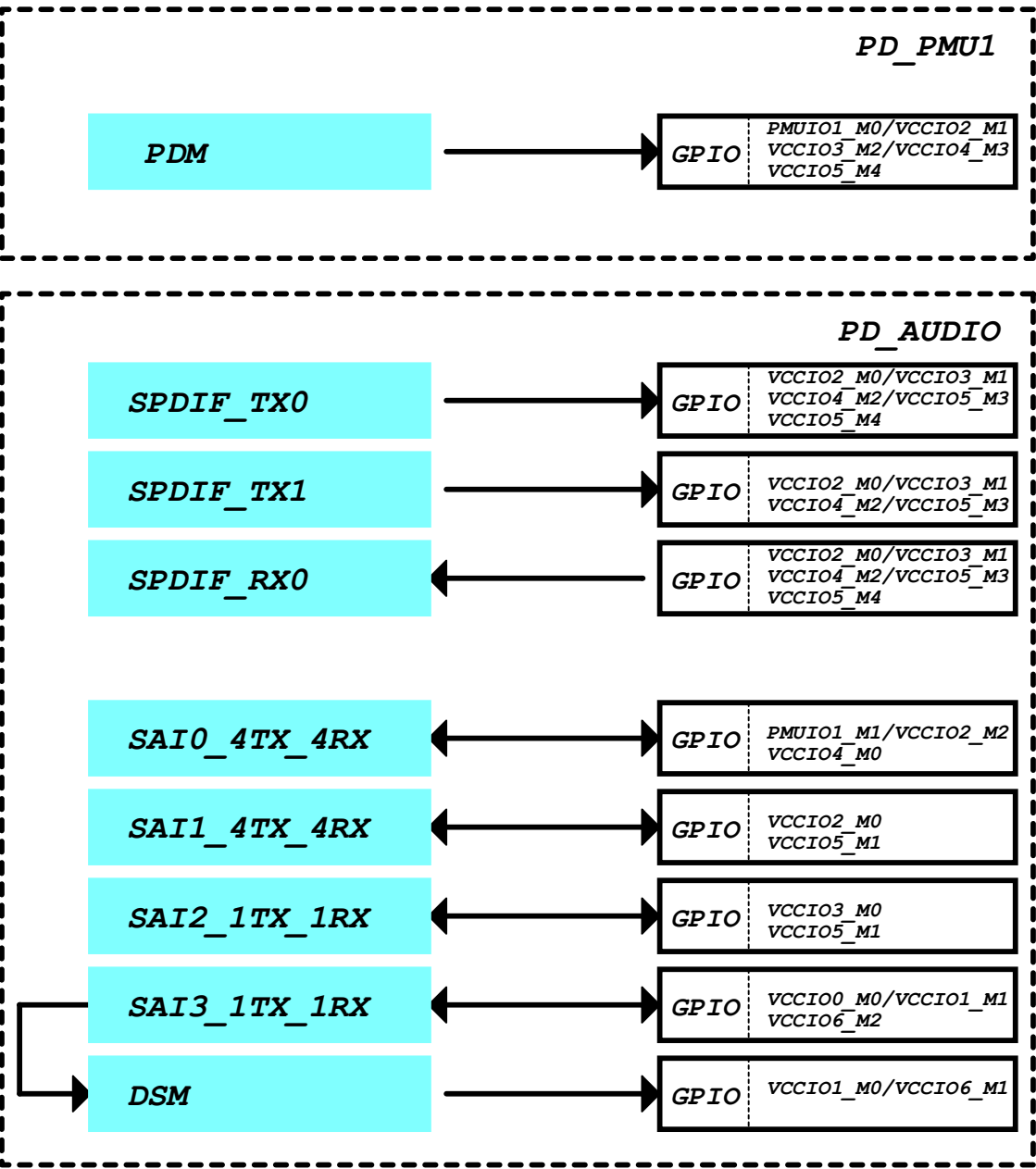
Unselected IOMUX path

IOMUX path in use

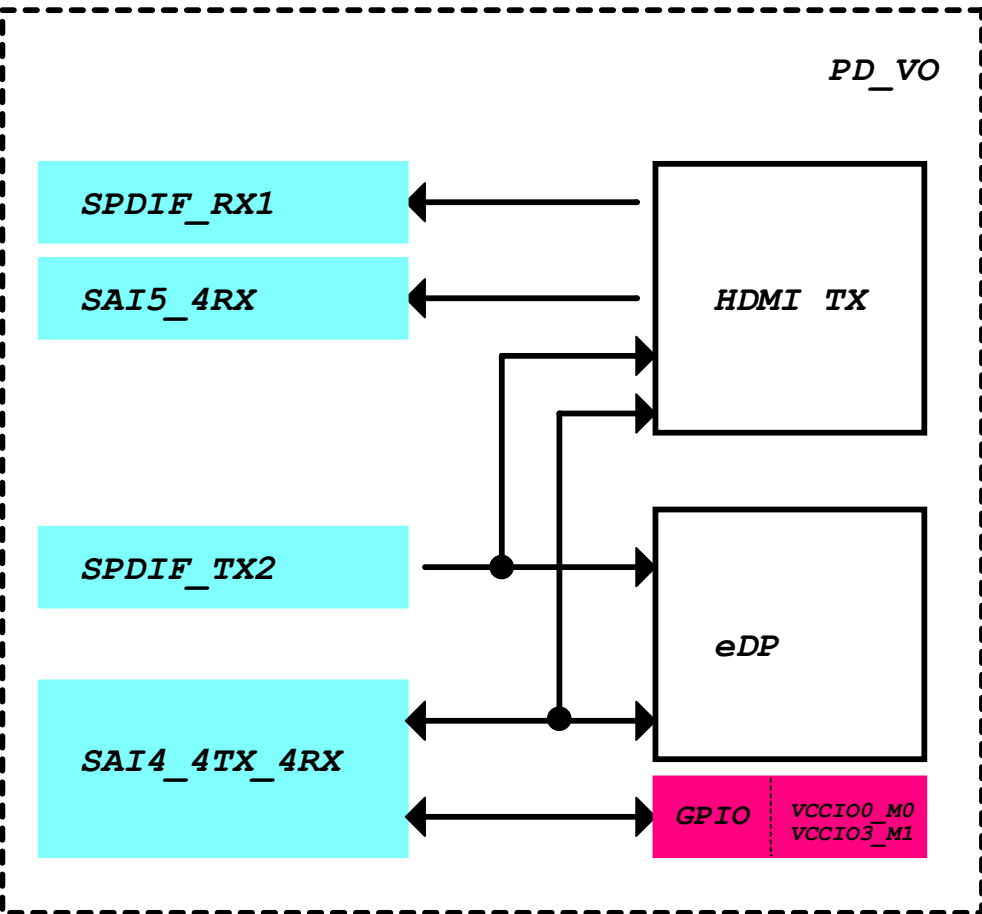
At the same time, only one path can be selected.

AUDIO MAP

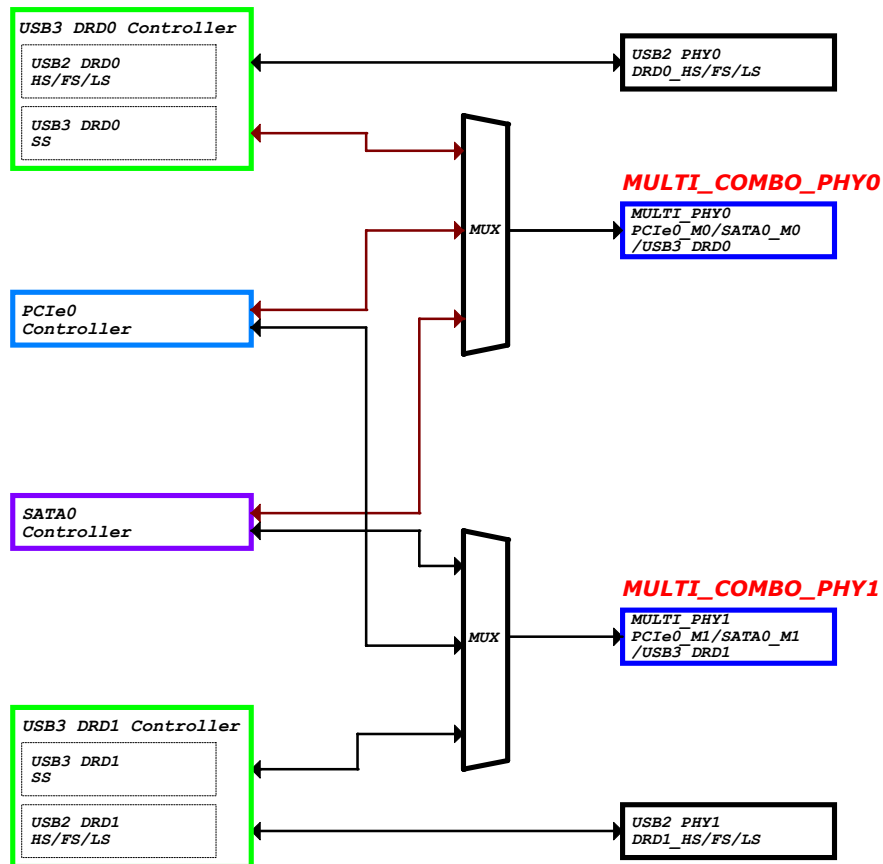
Chip Outernal



Chip Internal

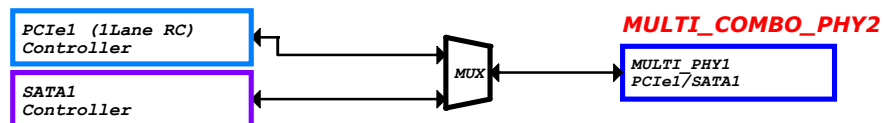


Note ! ! !
If HDMI/eDP function is used, SAI4 on the external GPIO cannot be used.

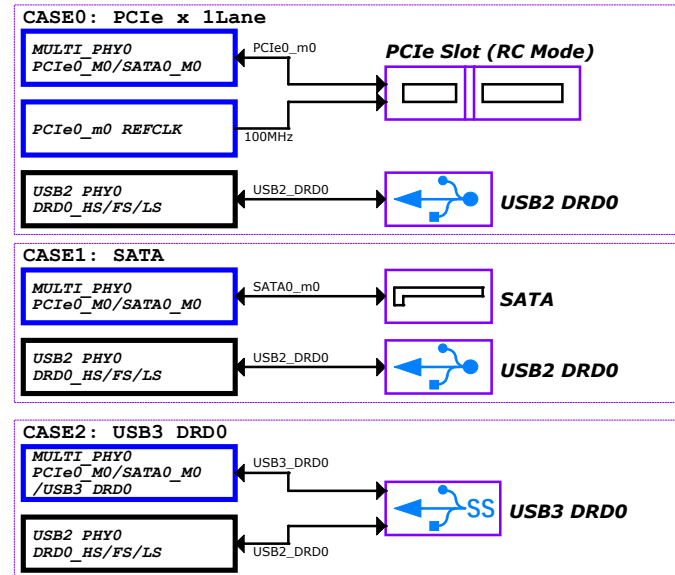


Note
PCIe port no support EP mode

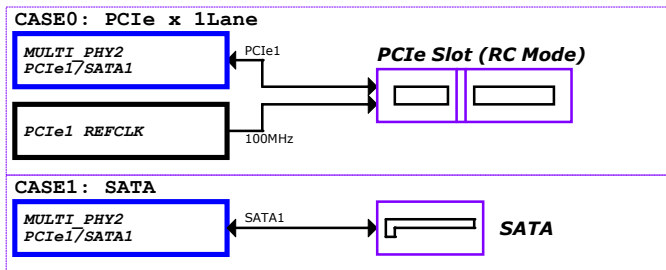
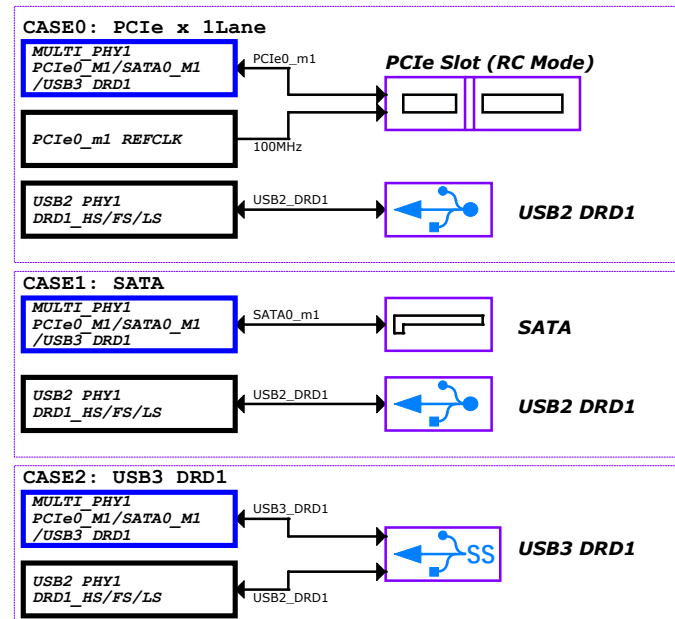
PCIe Combo PHY2--PCIe1/SATA1



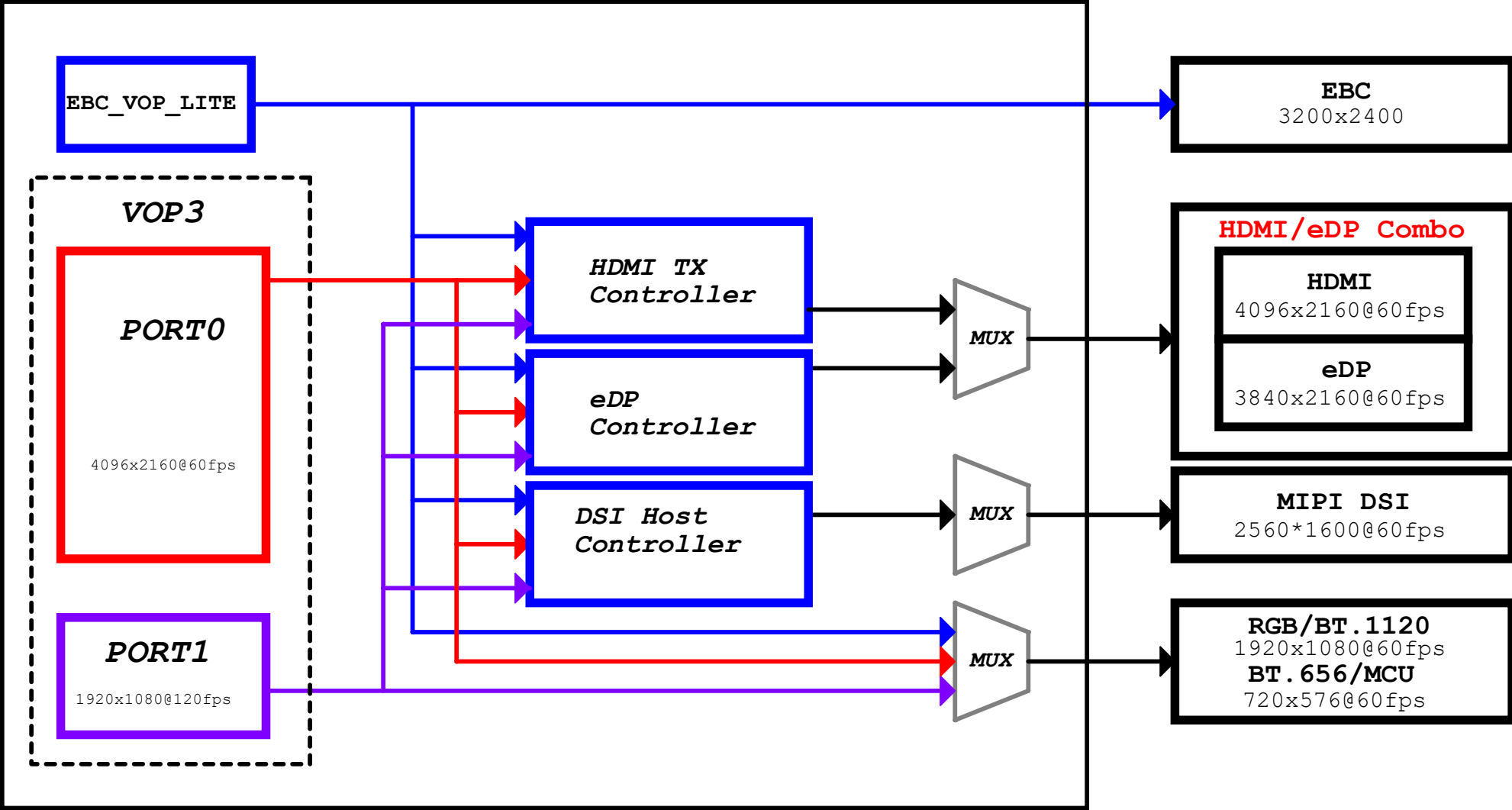
MULTI_COMBO_PHY0 PCIe0_m0/SATA0_m0 USB3 DRD0



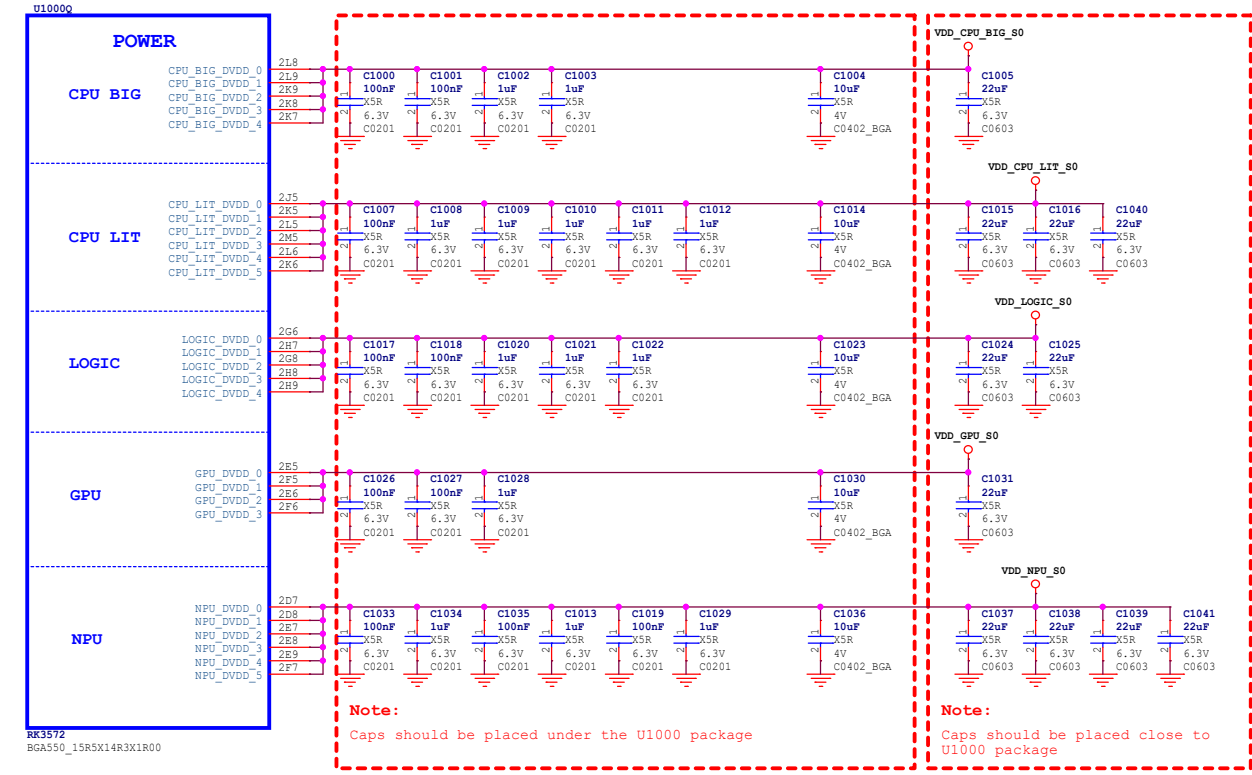
MULTI_COMBO_PHY1 PCIe0_m1/SATA0_m1 USB3 DRD1



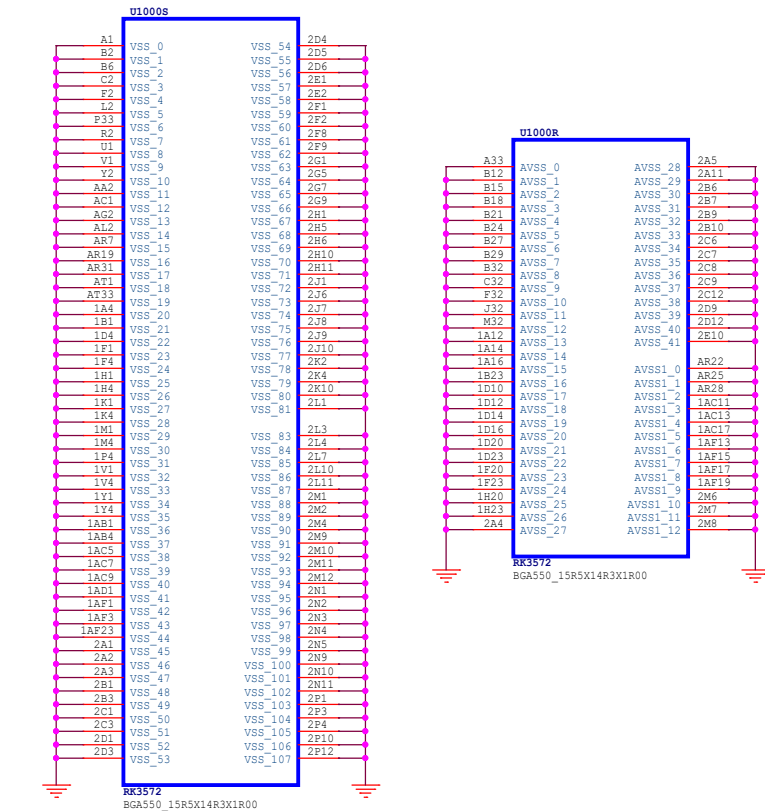
VO MAP



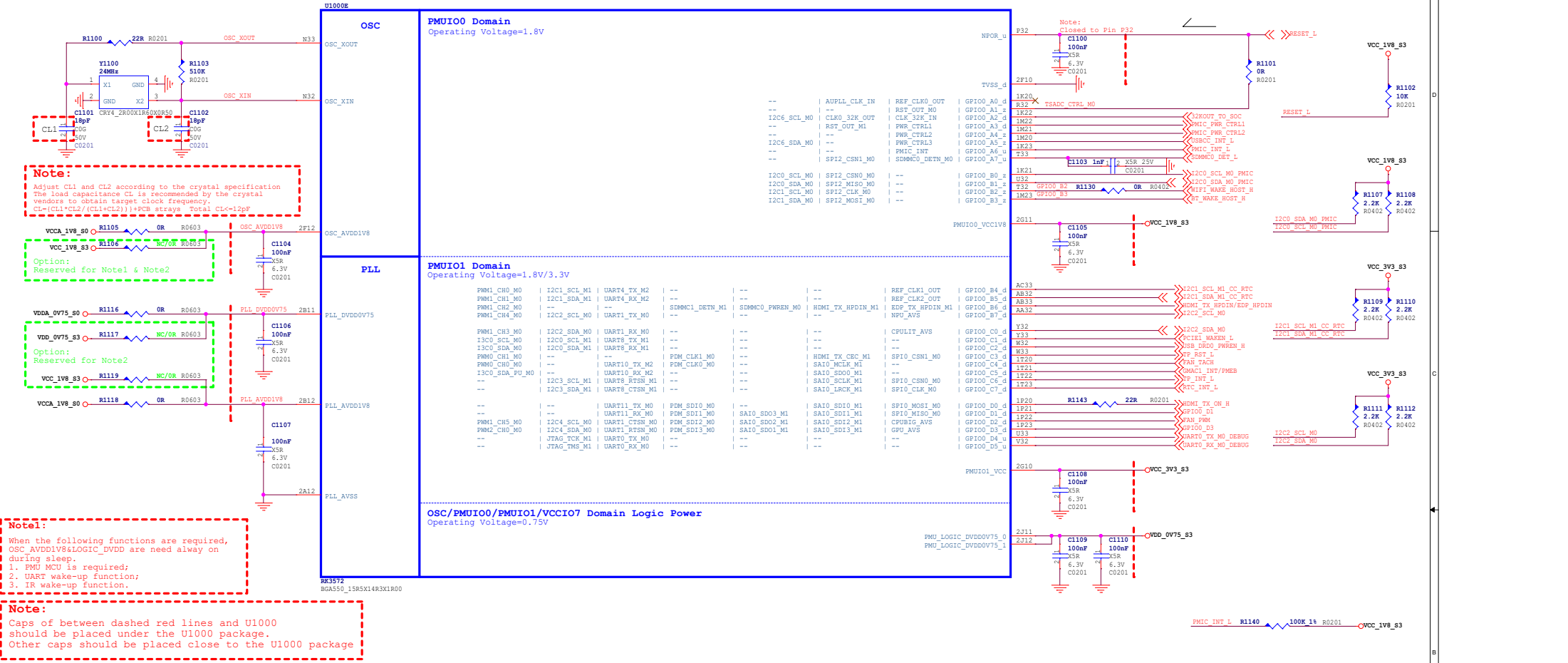
RK3572_Q (Power)



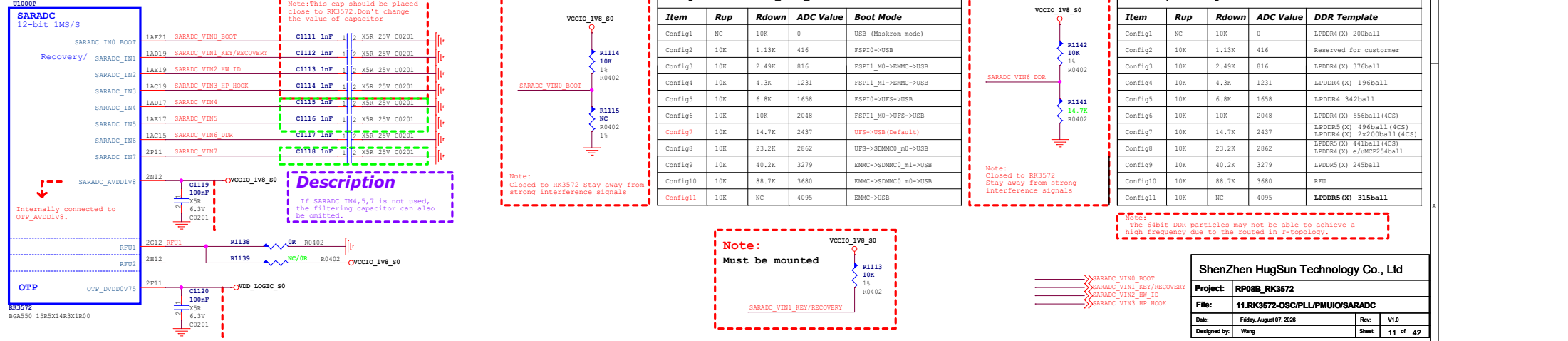
RK3572_S/R (GND)



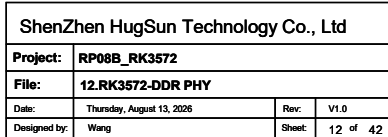
RK3572_E (PMUIO0/1)



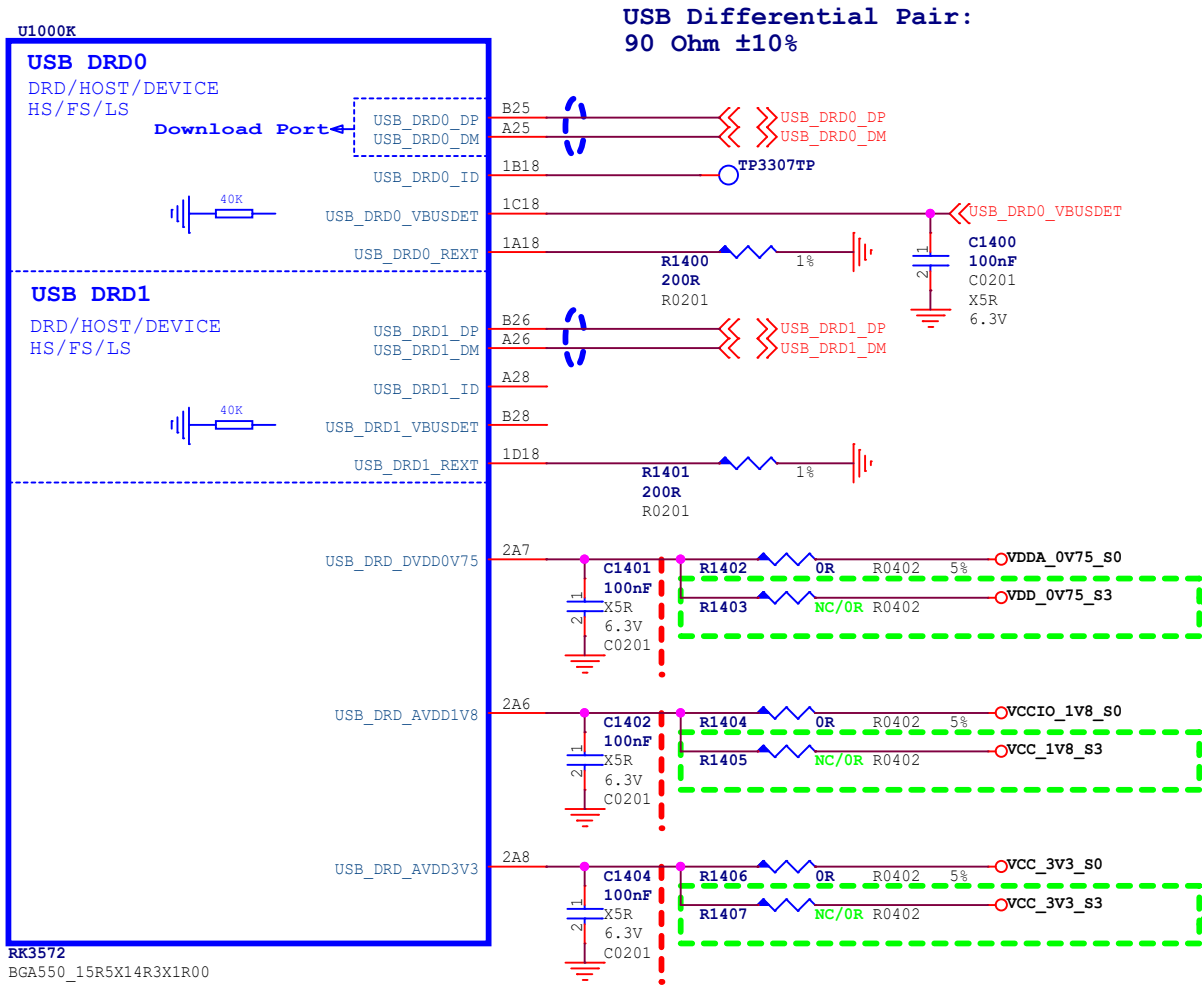
RK3572_P (SARADC)



LPDDR4/4X LPDDR5/5X



RK3572_K (USB2)



Note:
USB2_DRD0_ID:
There is an internal pull-up resistor connected to 1.8V

Note:
USB20_DRD*_VBUSDET:
Internal has a pull-down resistance (40K ohm) to ground.
The VBUSDET pin voltage range <=3.3V.

OPTION
Reserved for USB wake up

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

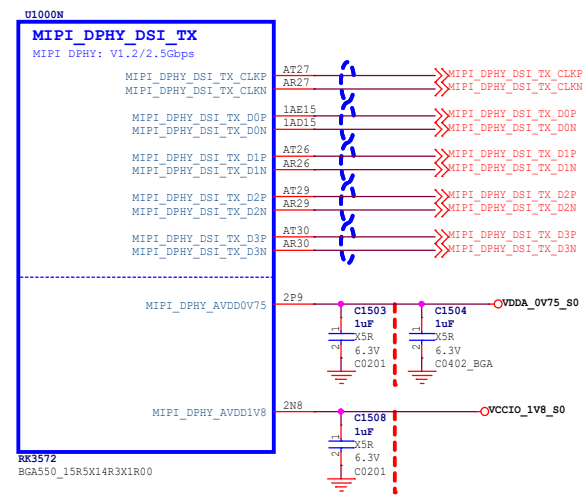
Note:
USB2_OTG0:
DP/DM :Must be used for download
ID :According to demand, if not used, leave floating
VBUSDET:Must be used for download
REXT :200ohm 1% resistor must be connected externally
Power :Must supply power
USB2_OTG1:
If not used:
DP/DM :Leave floating
ID :Leave floating
VBUSDET:Leave floating
REXT :Leave floating

ShenZhen HugSun Technology Co., Ltd			
Project:	RP08B_RK3572		
File:	14.RK3572-USB2		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	14 of 42

RK3572_N
(MIPI DPHY DSI TX)

Note:
MIPI DPHY supports up to 2560 x 1600@60Hz
Support 1/2/4Lane

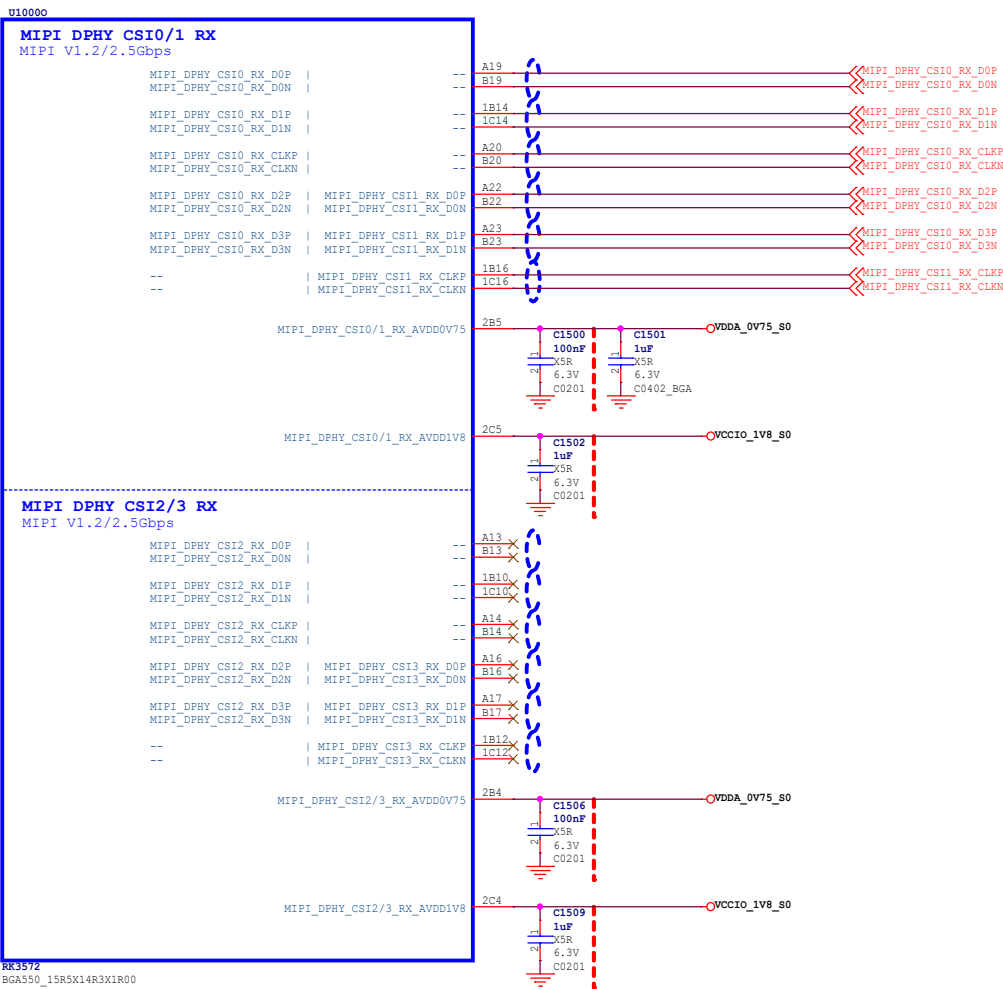
MIPI DSI TX Differential Pair:
100 Ohm $\pm 10\%$



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If not used:
Signal: Leave floating
Power : Tie to VSS

RK3572_O (MIPI DPHY CSI RX)



MIPI_DPHY_CSI0/1_RX Configuration

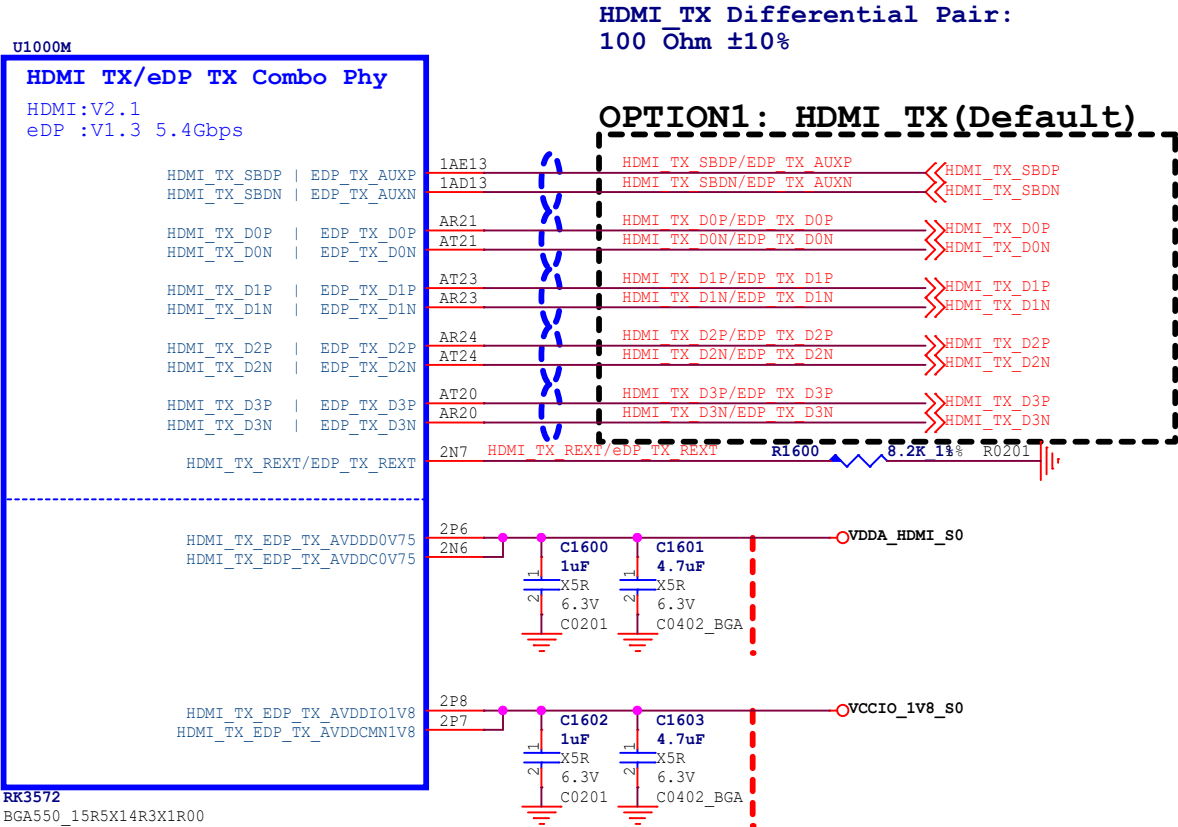
Option1	Sensor1 x4Lane	MIPI_DPHY_CSI0_RX Lane0-Lane3 MIPI_DPHY_CSI0_RX_CLK
Option2	Sensor1 x2Lane	MIPI_DPHY_CSI0_RX Lane0-Lane1 MIPI_DPHY_CSI0_RX_CLK
	+ Sensor2 x2Lane	MIPI_DPHY_CSI1_RX Lane0-Lane1 MIPI_DPHY_CSI1_RX_CLK
Option3	Sensor1 x1Lane	MIPI_DPHY_CSI0_RX Lane0 MIPI_DPHY_CSI0_RX_CLK
	+ Sensor2 x1Lane	MIPI_DPHY_CSI1_RX Lane0 MIPI_DPHY_CSI1_RX_CLK

Note:
MIPI_DPHY_CSI*_RX: Support 1/2/4Lane
MIPI_DPHY_CSI2/3 RX Configuration is the same with MIPI_DPHY_CSI0/1_RX.

Note:
If not used:
Signal: Leave floating
Power : Leave floating or tie to VSS

RK3572_M (HDMI/eDP)

Note:
HDMI 2.1 supports up to 4096 x 2160@60Hz
Support 1/2/4Lane



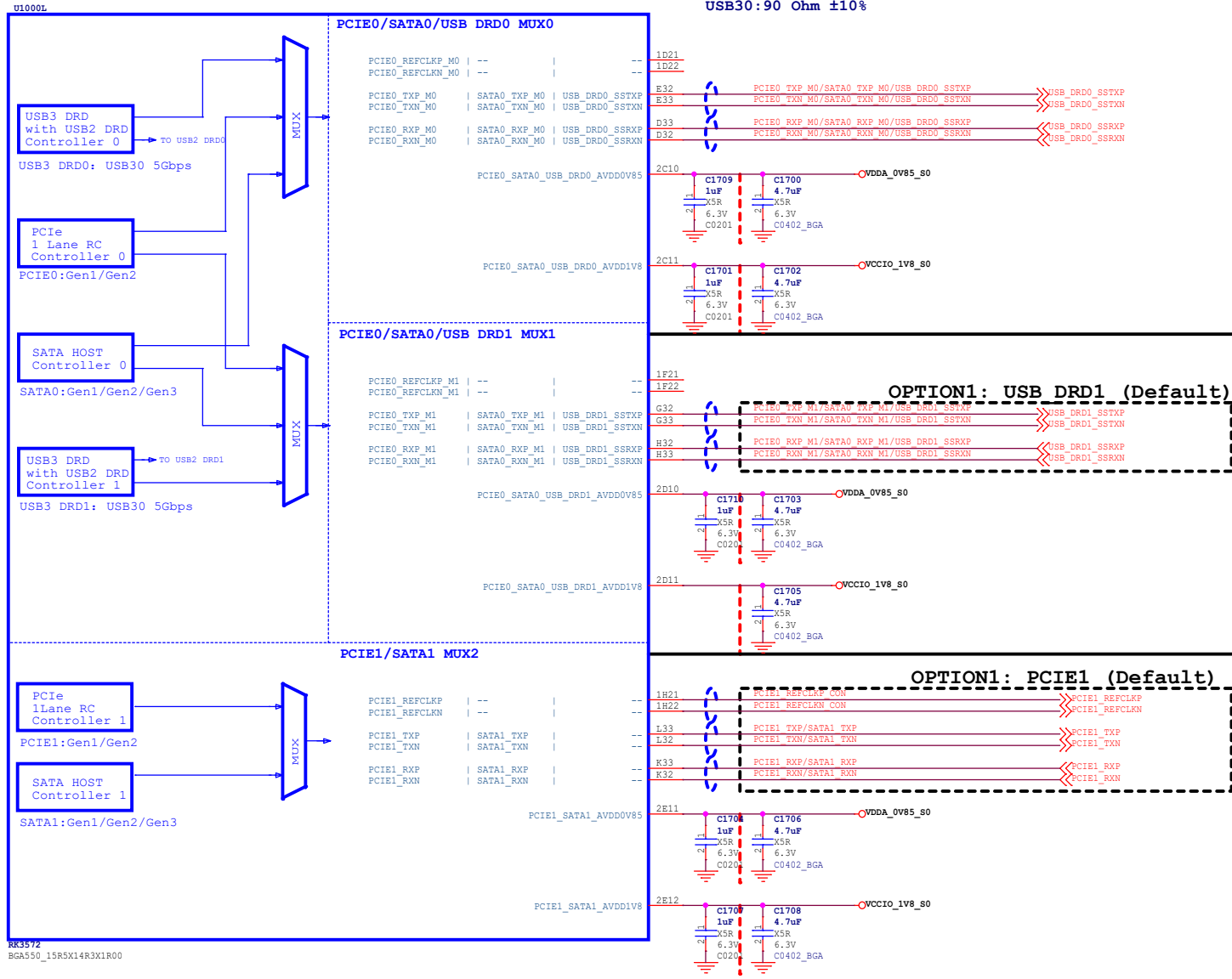
Note:
If not used:
Signal: Leave floating
Power : Leave floating or tie to VSS

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

ShenZhen HugSun Technology Co., Ltd			
Project:	RP08B_RK3572		
File:	16.RK3572-HDMI/eDP		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	16 of 42

RK3572_L (PCIe/USB3)

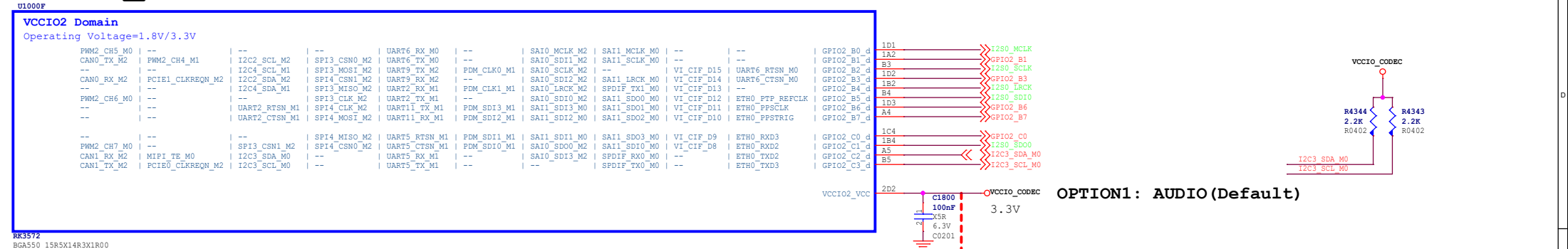
PCIe/SATA/USB Differential Pair:
CLK: 100 Ohm $\pm 10\%$
SATA: 100 Ohm $\pm 10\%$
PCIe: 85 Ohm $\pm 10\%$
USB30: 90 Ohm $\pm 10\%$



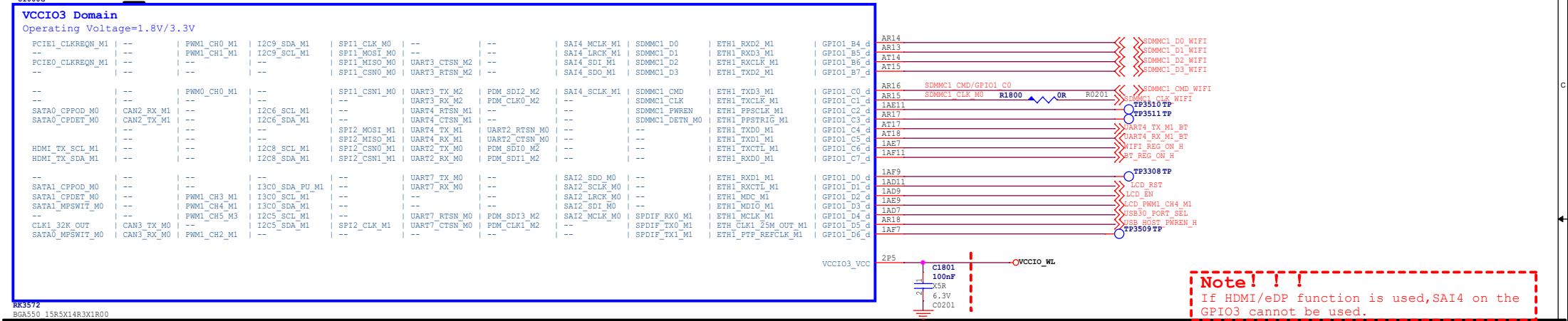
Note:
If not used:
Signal: Leave floating
Power : Tie to VSS

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

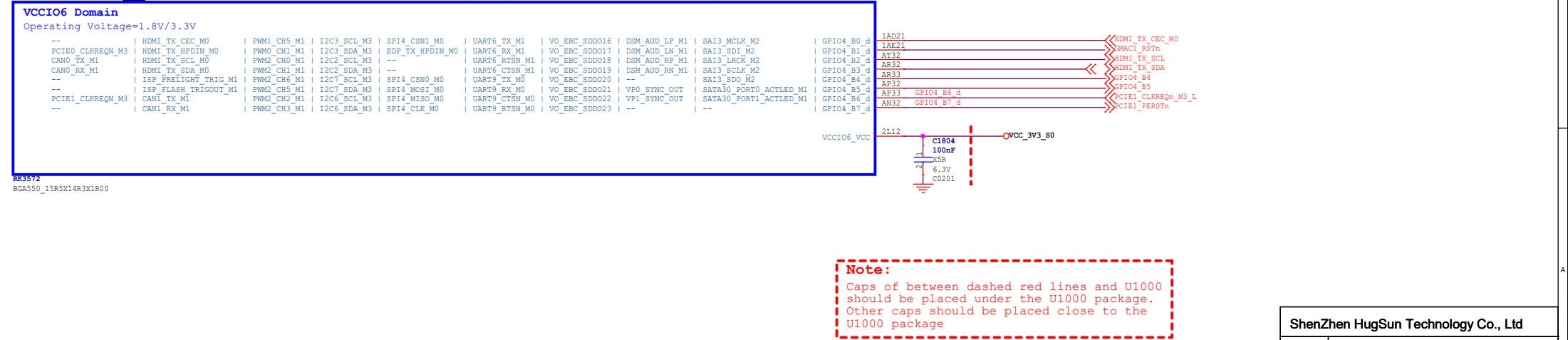
RK3572_F (VCCIO2)



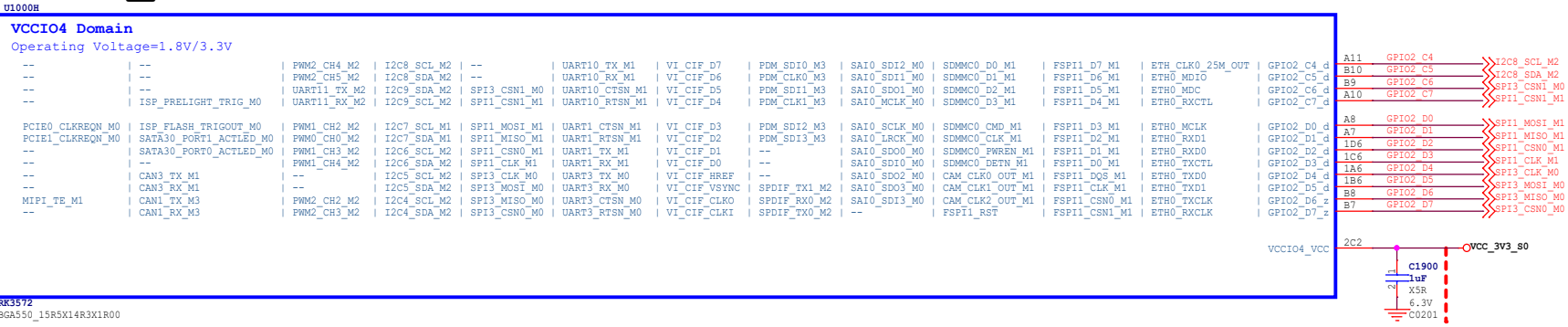
RK3572_G (VCCIO3)



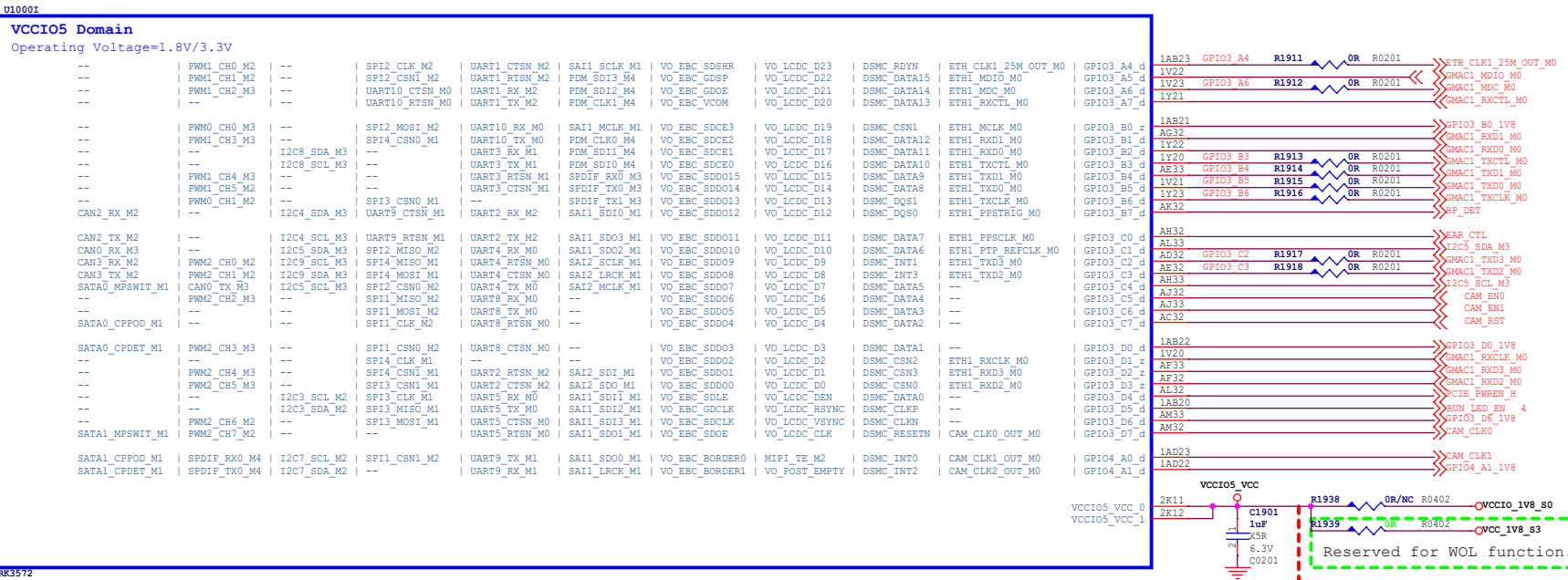
RK3572_J (VCCIO6)



RK3572_H (VCCIO4)



RK3572_I (VCCIO5)

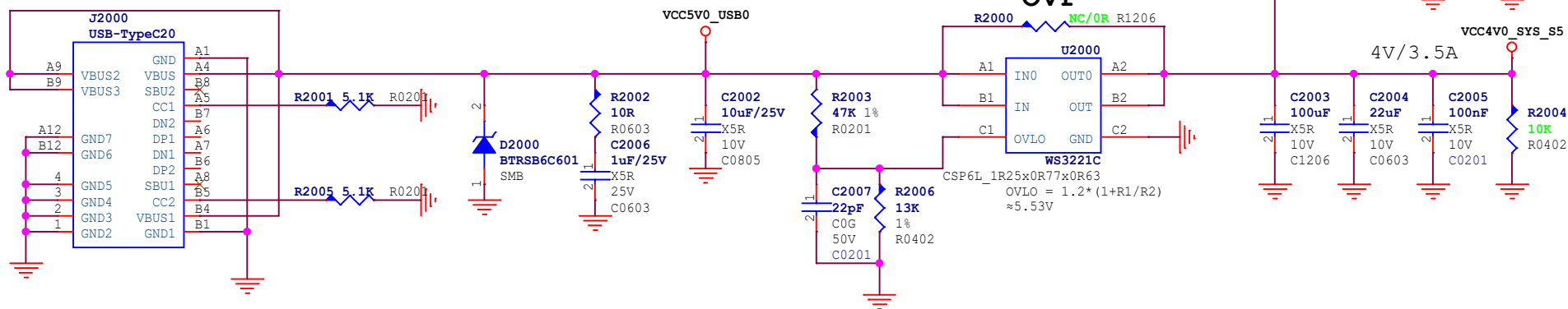


Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

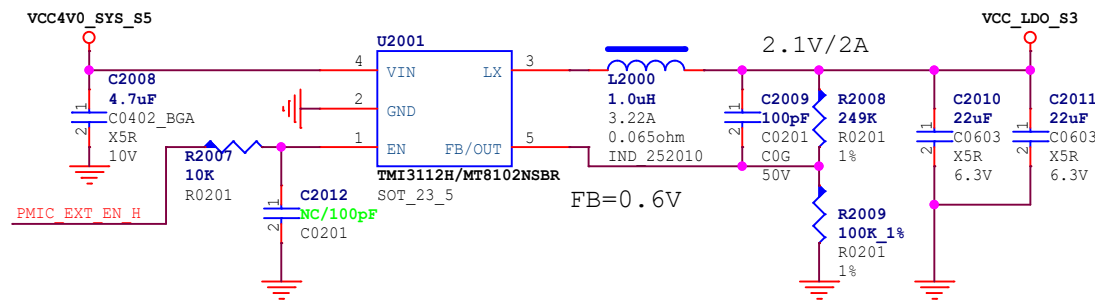
ShenZhen HugSun Technology Co., Ltd				
Project:	RP08B_RK3572			
File:	19.RK3572-GPIO VCCIO4/5			
Date:	Friday, August 07, 2026	Rev:	V1.0	
Designed by:	Wang	Sheet:	19 of 42	

PMIC_EXT_EN_H

Type-c 5V



VCC_LD0IN_S3



ShenZhen HugSun Technology Co., Ltd

Project:	RP08B_RK3572		
File:	20.Power-DC IN		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	20 of 42

PMIC RK806-5 BUCK



Description:
VDD_NPU_S0 → R2344 → VDD_CPU_S0
R0805

In some scenarios, NPU and GPU can be combined. If do so, BUCK5 can be reserved for the "VCC_LDO_S3" power rail.

Default: 0.75V

Power Name	Voltage	Ru
VDD_CPU_S0	0.75V	49.9K 1%
VCC_LDO_S3	2.1V	100K 1%

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Voltage: 5.5V
Peak Pulse Current (8/20us): 40A
Surge Clamping Voltage: 5.5V

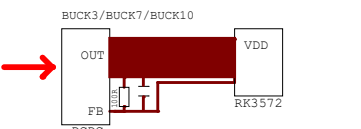
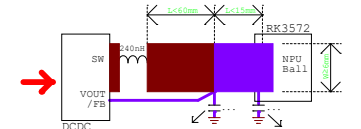
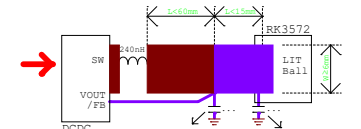
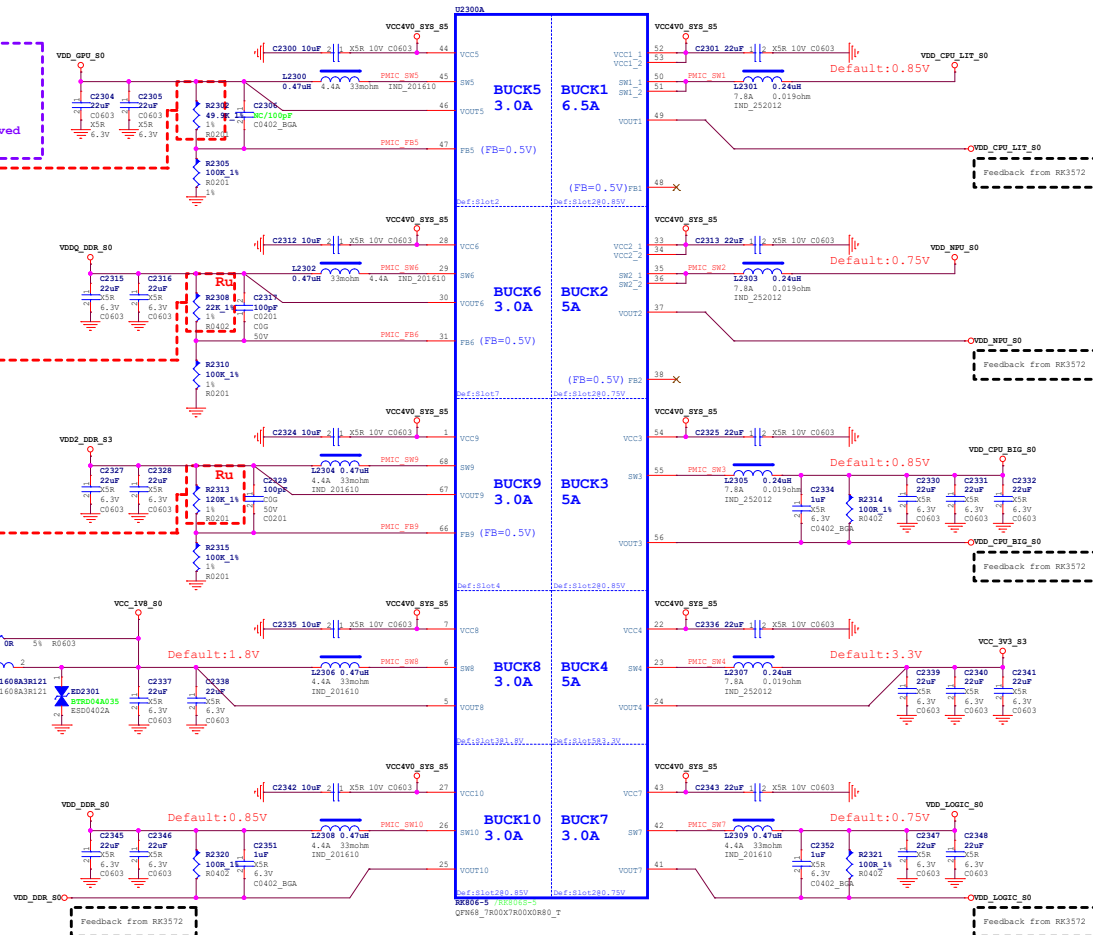
DO NOT DELETE IT!

Default: 0.51V

DRR Type	Voltage	Ru
LP00R5	0.51V	2.7K 1%
LP00R4	0.52V	2.7K 1%
LP00R4	0.76V	51K 1%

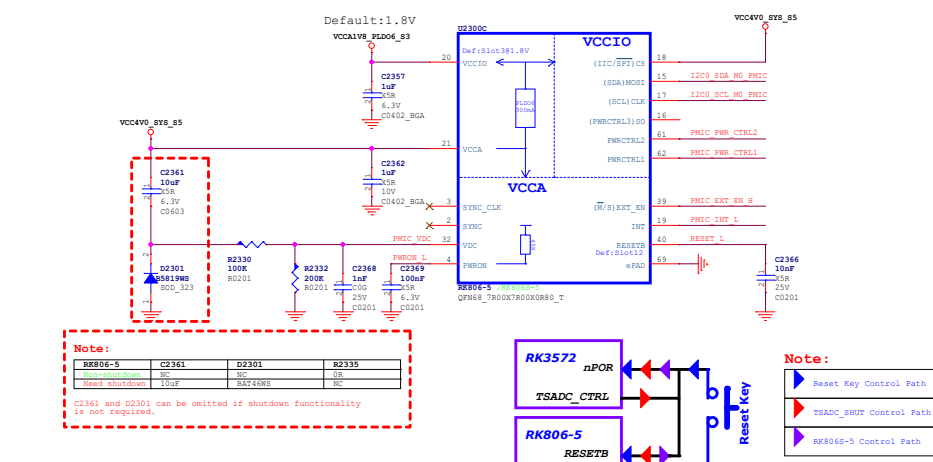
Default: 1.05V

DRR Type	Voltage	Ru
LP00R4/45	1.1V	120K 1%
LP00R5	1.05V	110K 1%



PMIC RK806-5 Managerment

Note:
I2C Mode: CS (pin18) connected to VCCA (pin21);
SPI Mode (Def): CS (pin18) floating or connected to GND

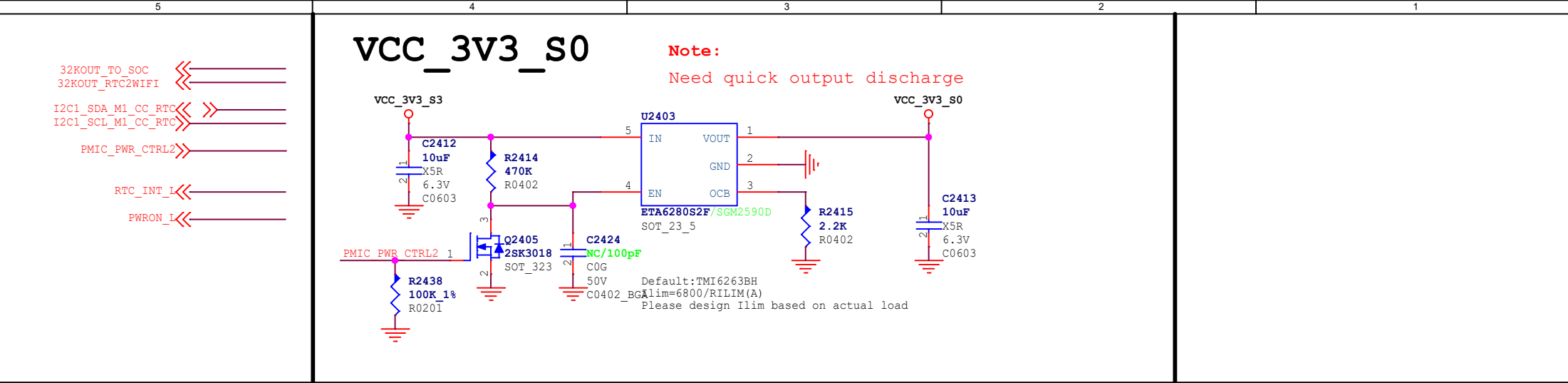


PMIC RK806-5 LDO



The "VDDA HDMI_S0" power rail must be adjusted from 0.75V to 0.8375V after power on.

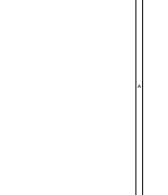
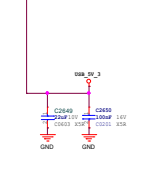
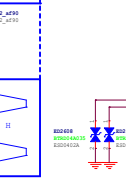
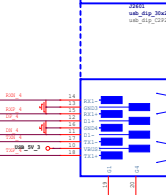
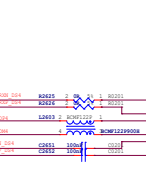
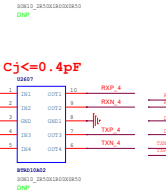
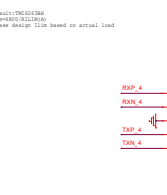
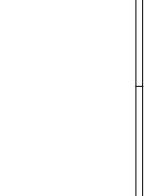
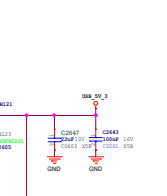
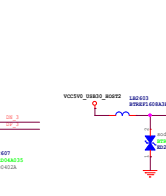
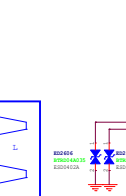
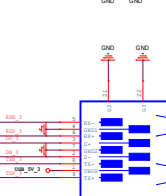
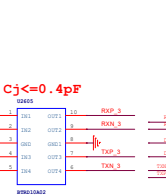
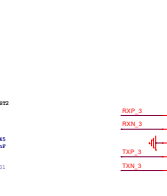
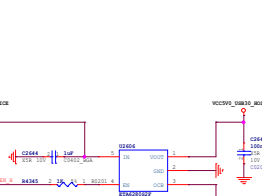
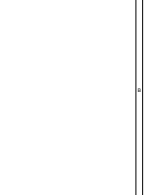
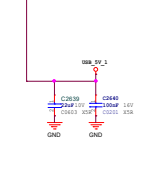
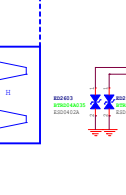
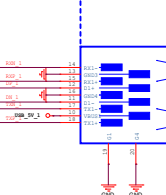
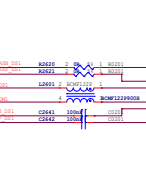
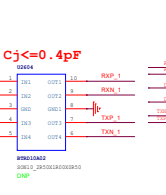
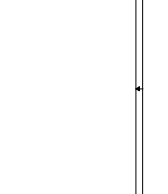
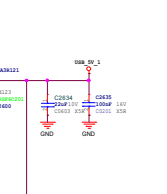
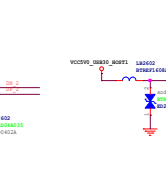
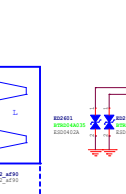
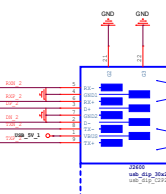
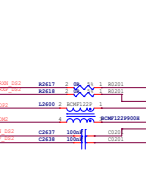
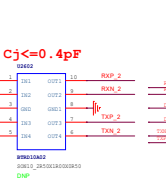
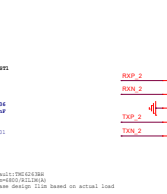
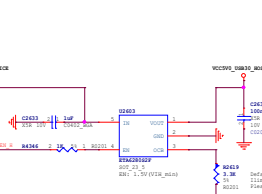
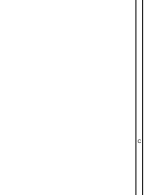
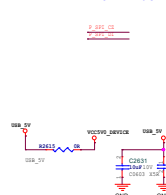
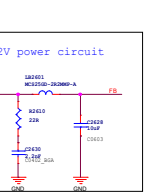
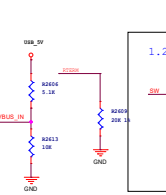
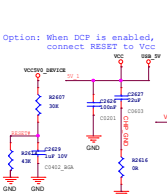
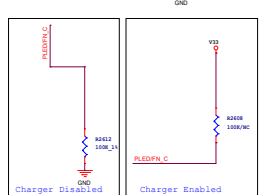
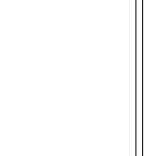
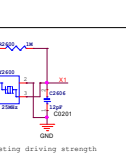
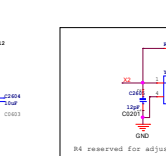
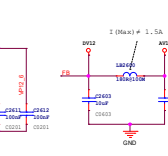
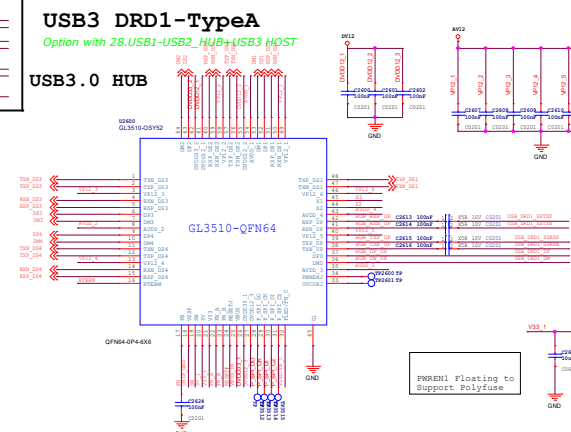
Note:
The RK806 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re-evaluated, otherwise the added functions may exceed the maximum current provided by the LDO.



USB3 DRD1-TypeA

Option with 28.USB1-USB2_HUB+USB3 HOST

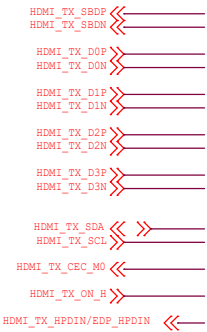
USB3.0 HUB



ShenZhen HugSun Technology Co., Ltd	
Project:	RP08B1-NC3572
File:	28.USB1-TYPEA USB3.0
Date:	2019, August 07, 2019
Designer:	Wang
Rev:	1.0
Page:	26 of 42

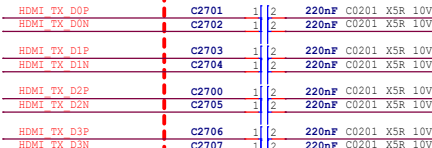
HDMI 2.1

Option with 53.VO-LCM eDP TX(Optional)



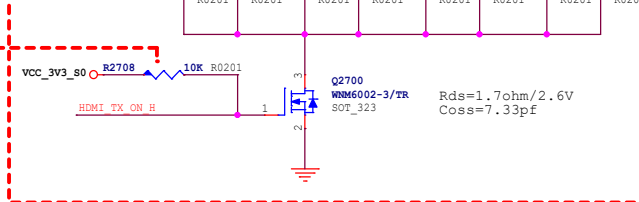
Note:

Close to HDMI Connector



Note:

Close to HDMI Connector



Note:

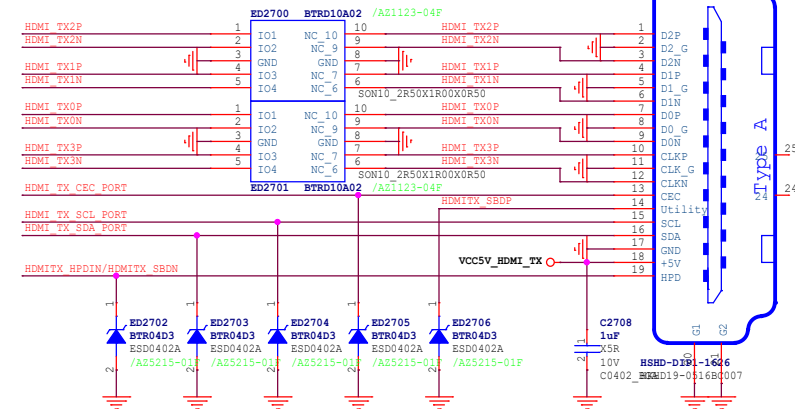
The controller only support AC coupled link.
In order to backward compatibility or to meet HDMI2.0 (1.4b)
DC common mode spec and Voff, need do R based level-shift.

Support video output up to 4096 x 2160@60Hz

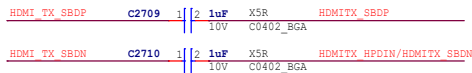
Note:

The Cj of ESD must<=0.2pf

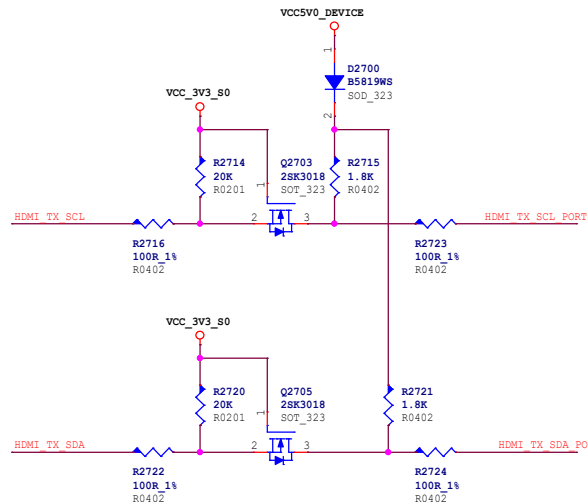
AZ1123-04F
Vbr<10V
Vcl=7.5V
Cj<0.3p



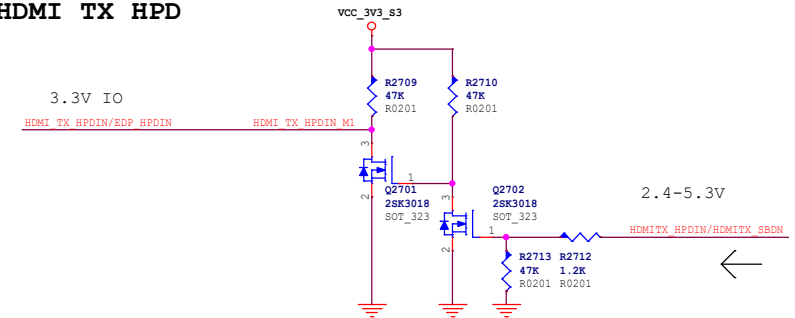
HDMI TX ARC



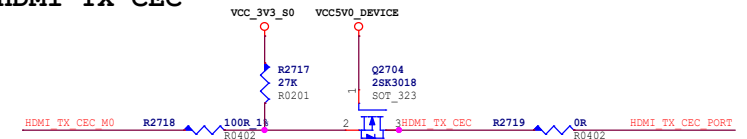
HDMI TX DDC



HDMI TX HPD



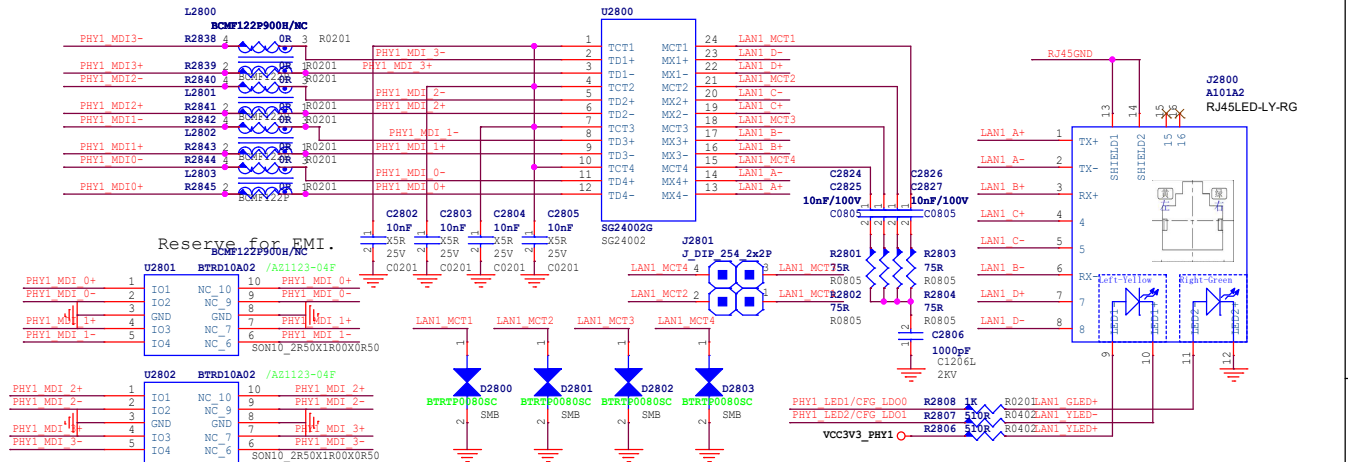
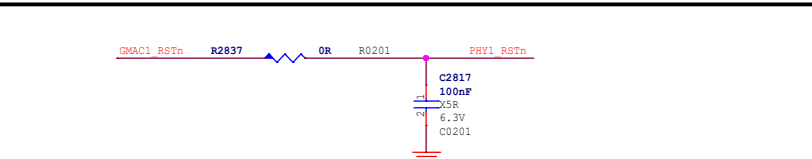
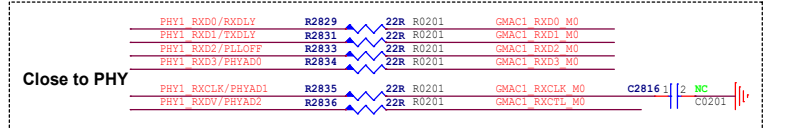
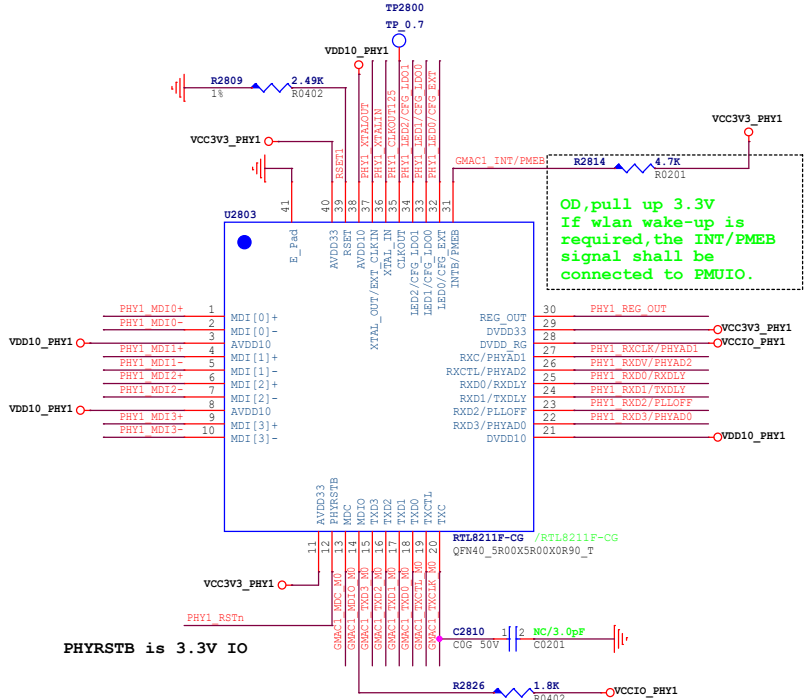
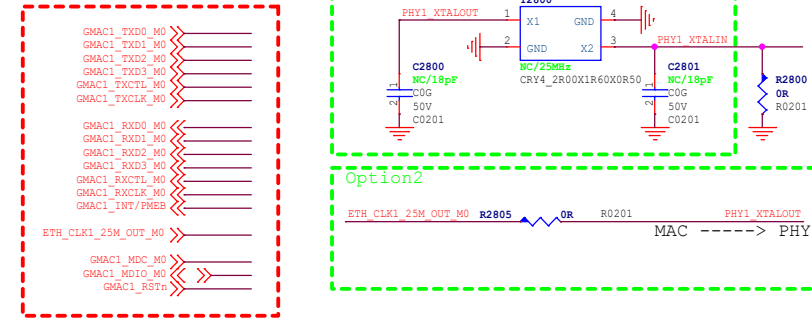
HDMI TX CEC



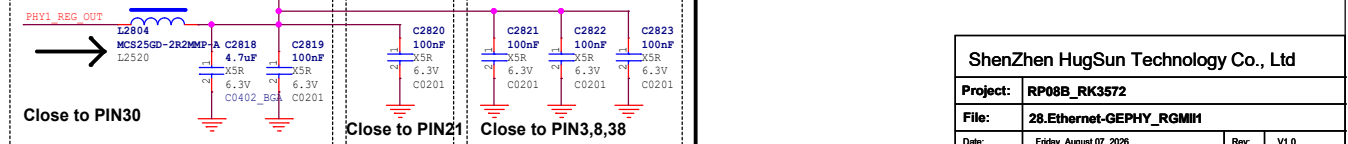
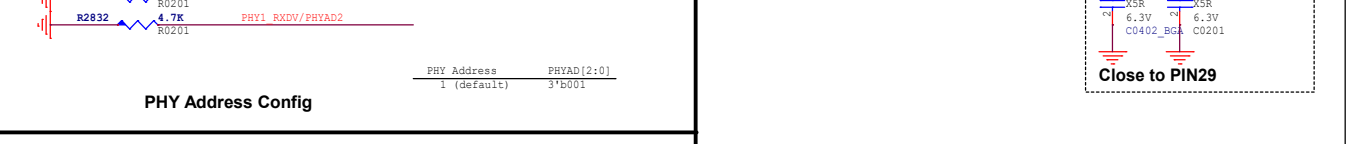
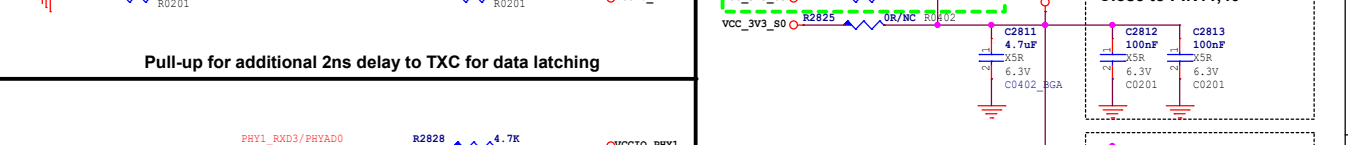
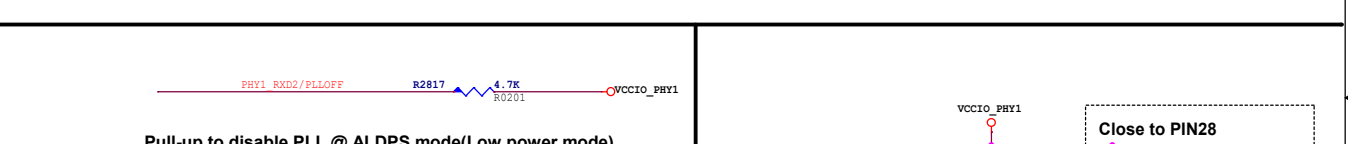
ShenZhen HugSun Technology Co., Ltd

Project:	RP08B_RK3572		
File:	27.VO-HDMI TX		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	27 of 42

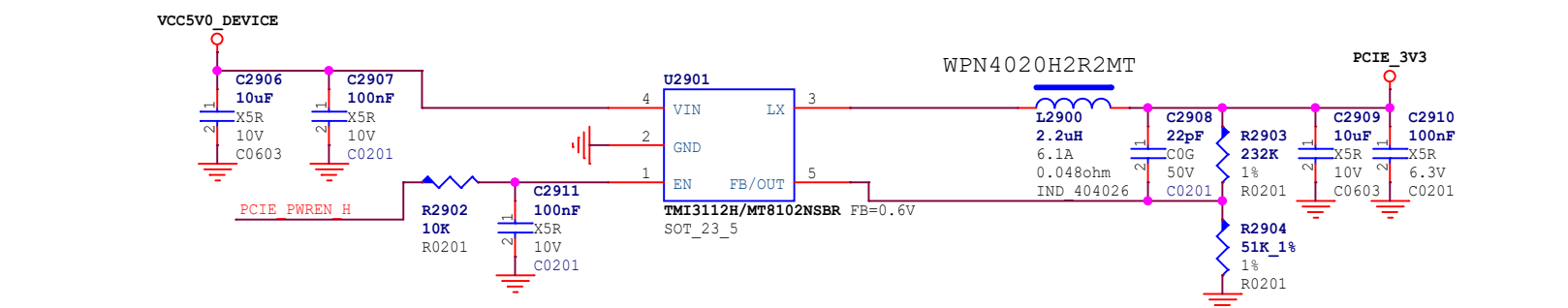
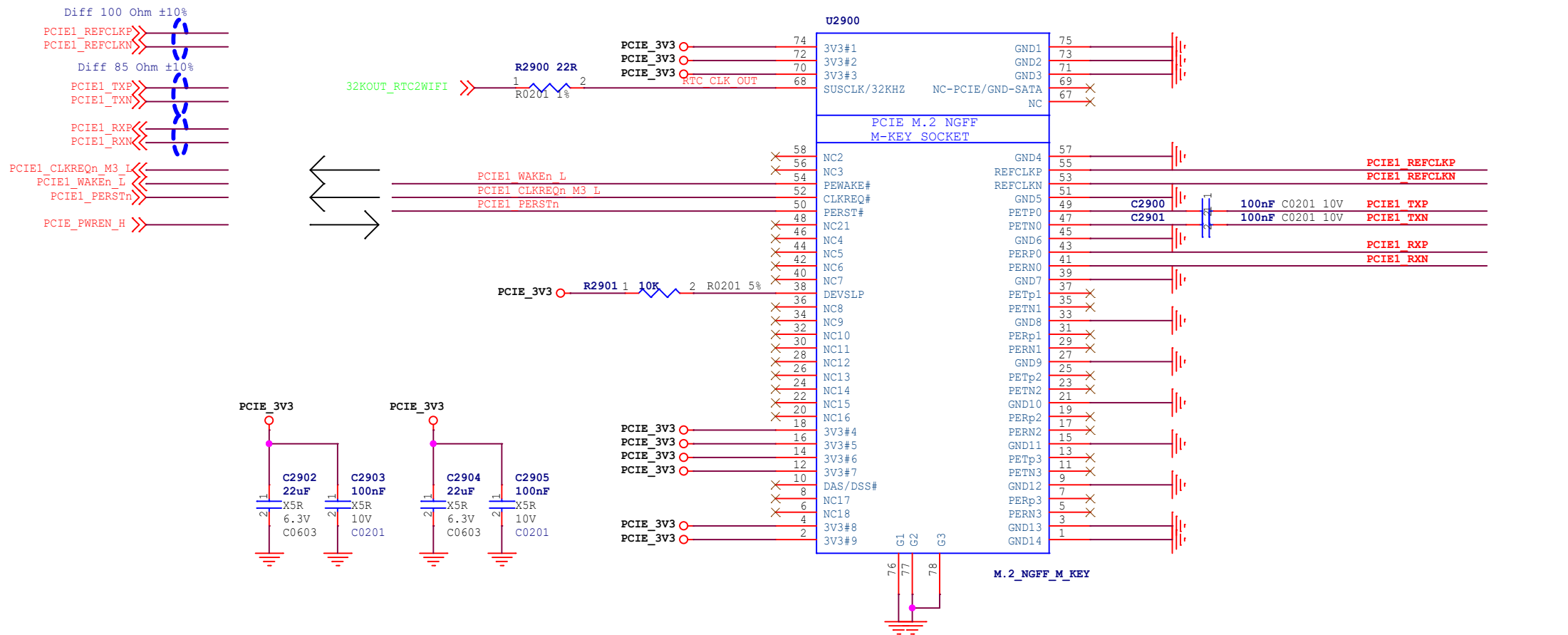
RGMI11_M0



VCC_PHY0_IO Voltage Config			
RGMI1 Power Source	CFG_EXT	CFG_LDO1[1:0]	CFG_EXT:
External 3.3V	1'b1	2'b00	1: External Power Source for IO pad.
External 1.8V	1'b1	2'b10	0: Integrated LDO for IO pad
Internal 1.8V(default)	1'b0	2'b10	CFG_LDO1(1:0) 10:1.8V 00:3.3V



ShenZhen HugSun Technology Co., Ltd			
Project:	RP08B_RK3572		
File:	28.Ethernet-GEPHY_RGMI11		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	28 of 42

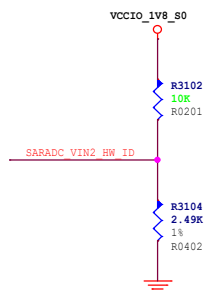


ShenZhen HugSun Technology Co., Ltd			
Project:	RP08B_RK3572		
File:	29.M.2 PCIE		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	29 of 42

Revision History

Version	Date	By	Change Dscription	Approved
V1.0	2026-06-05	Wangzhihai	1.REF designer by AIOT V1.1	

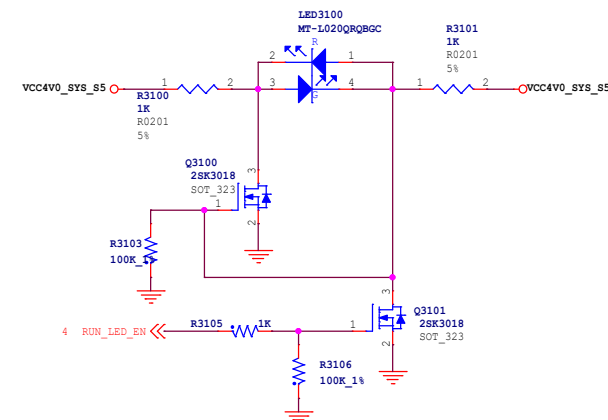
HW_ID



Config Table for SARADC_VIN2_HW_ID

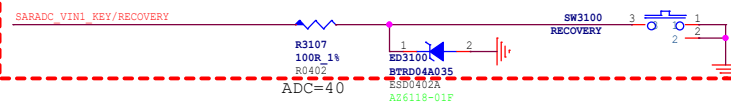
Item	Rup	Rdown	ADC Value	VERSION
HW_ID1	NC	10K	0	V1.0
HW_ID2	10K	1.13K	416	For Customer-Defined
HW_ID3	10K	2.49K	816	For Customer-Defined
HW_ID4	10K	4.3K	1231	For Customer-Defined
HW_ID5	10K	6.8K	1658	For Customer-Defined
HW_ID6	10K	10K	2048	For Customer-Defined
HW_ID7	10K	14.7K	2437	For Customer-Defined
HW_ID8	10K	23.2K	2862	For Customer-Defined
HW_ID9	10K	40.2K	3279	For Customer-Defined
HW_ID10	10K	88.7K	3680	For Customer-Defined
HW_ID11	10K	NC	4095	For Customer-Defined

POWER_LED



ARRAY KEY

SARADC_VIN1_KEY/RECOVERY
RESET_I
PWRON_I
SARADC_VIN0_BOOT



Note:
Please reserve this circuit
if the RECOVERY Key is not kept

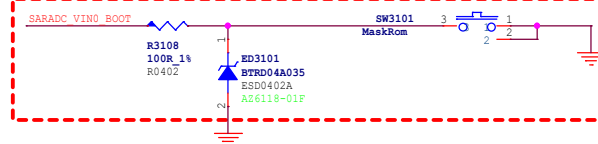
Description

It is suggested to reserve a
Key to facilitate the
development debug

If SARADC_VIN1=0V at after
power on and reset, then system
will enter into loader mode.

If there is no Key requirement,
two test points must be reserved
to facilitate firmware update

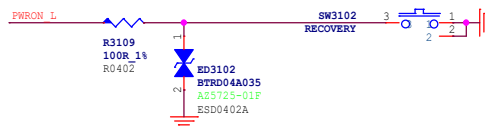
MASKROM Key



Note:
Please reserve this circuit
if the MASKROM_Key is not kept

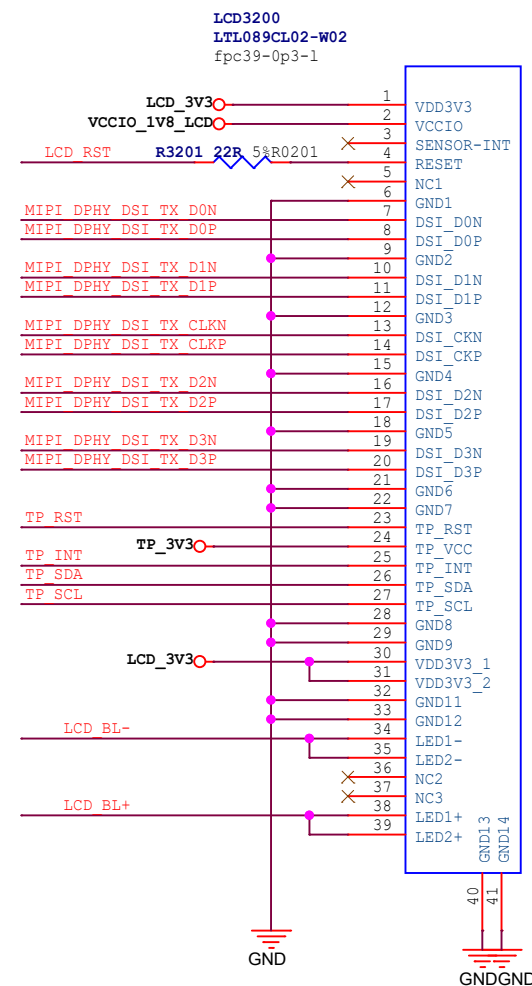
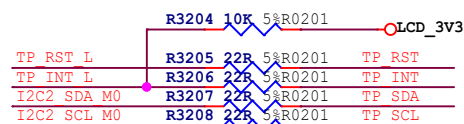
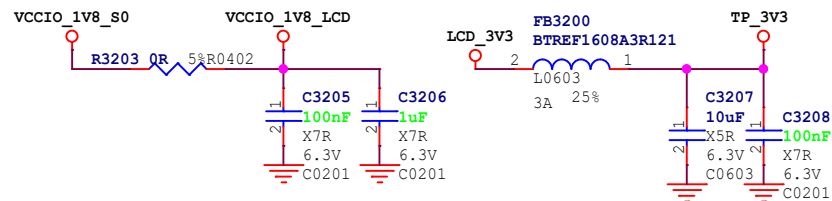
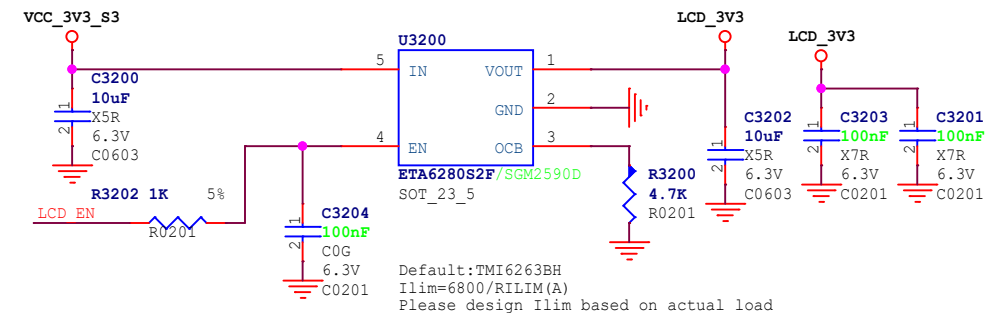
Description

If BOOT_SARADC_IN0=0V after power-on reset,
then system will enter into MASKROM mode.

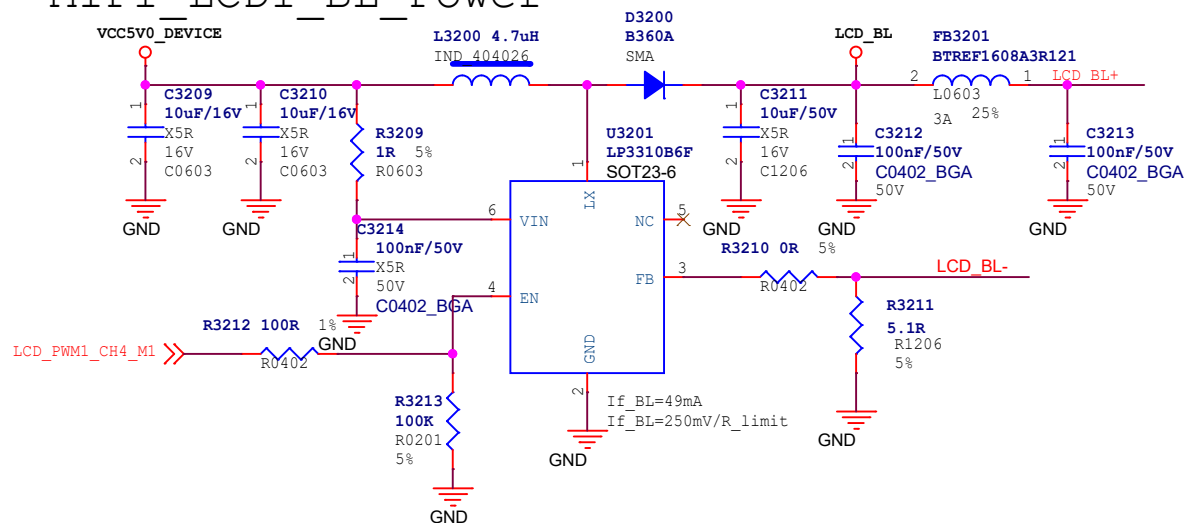


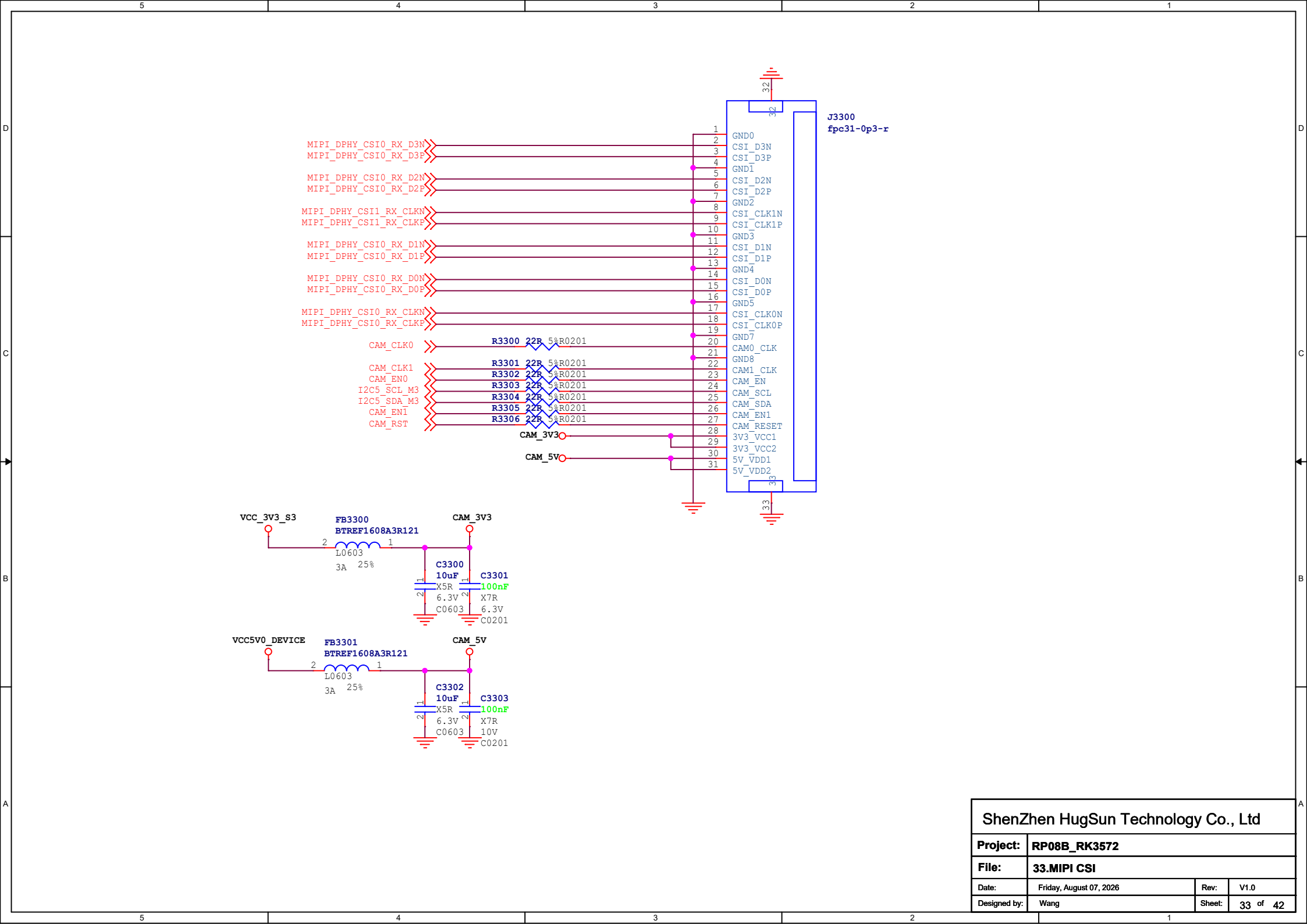
ShenZhen HugSun Technology Co., Ltd

Project:	RP08B_RK3572		
File:	31.HW_ID/LED/Key		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	31 of 42



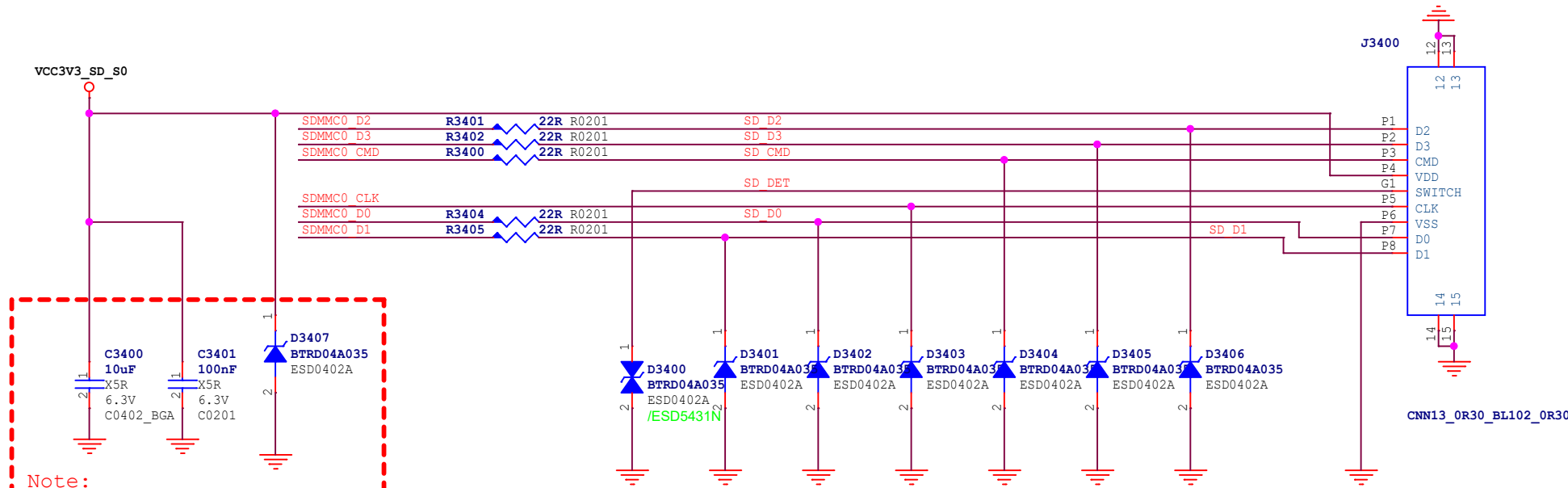
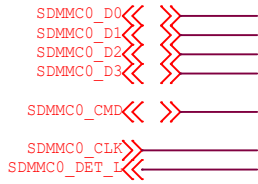
MIPI LCD1 BL Power





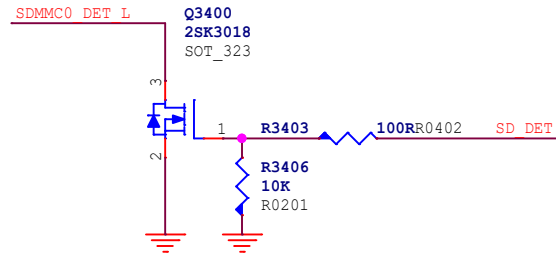
Project:	RP08B_RK3572		
File:	33.MIPI CSI		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	33 of 42

TF CARD



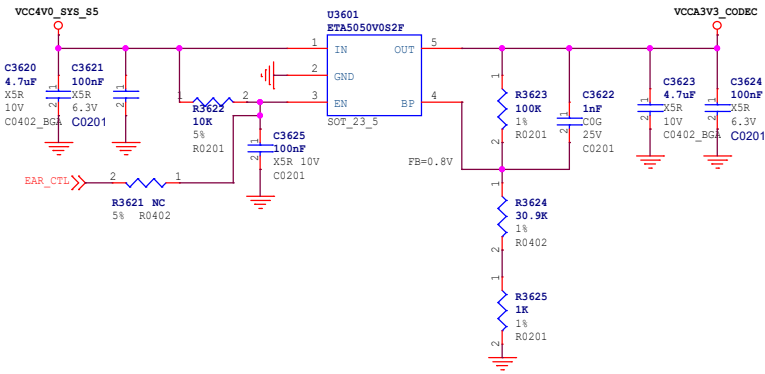
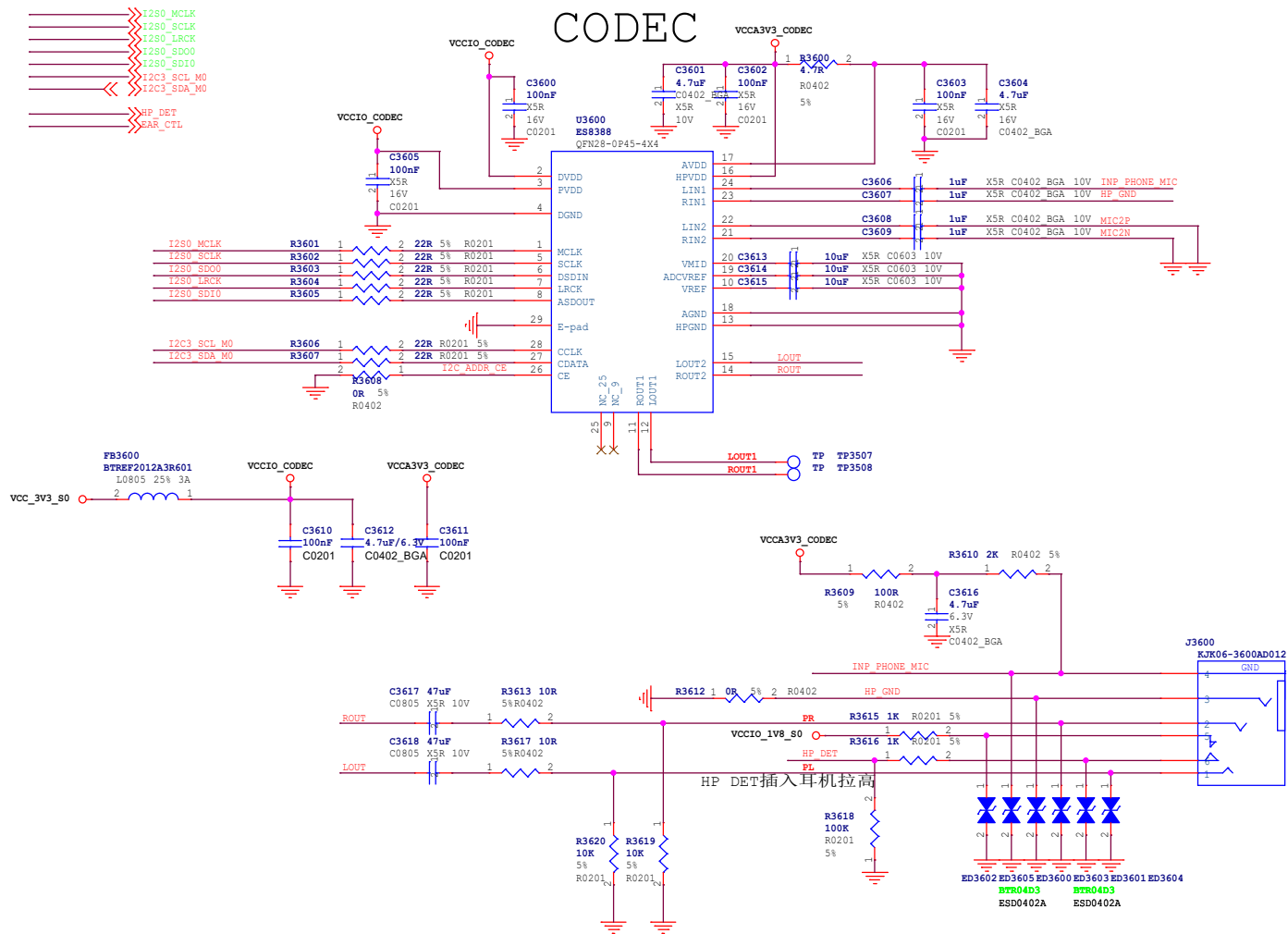
Note:
Close to MicroSD Card

Note:
SDMMC_DET_L:
SDCARD PLUG: Pull-down to GND
SDCARD UNPLUG: Pull-up to PMUIO0_VCC1V8.

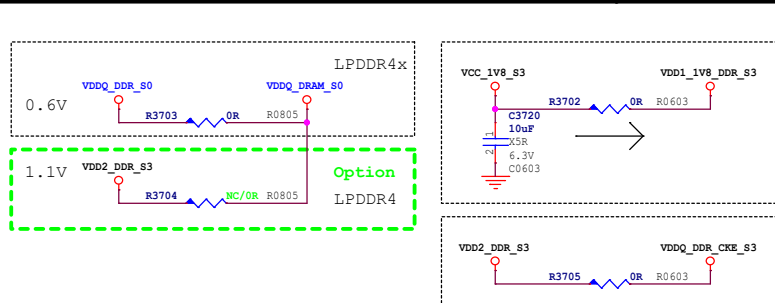
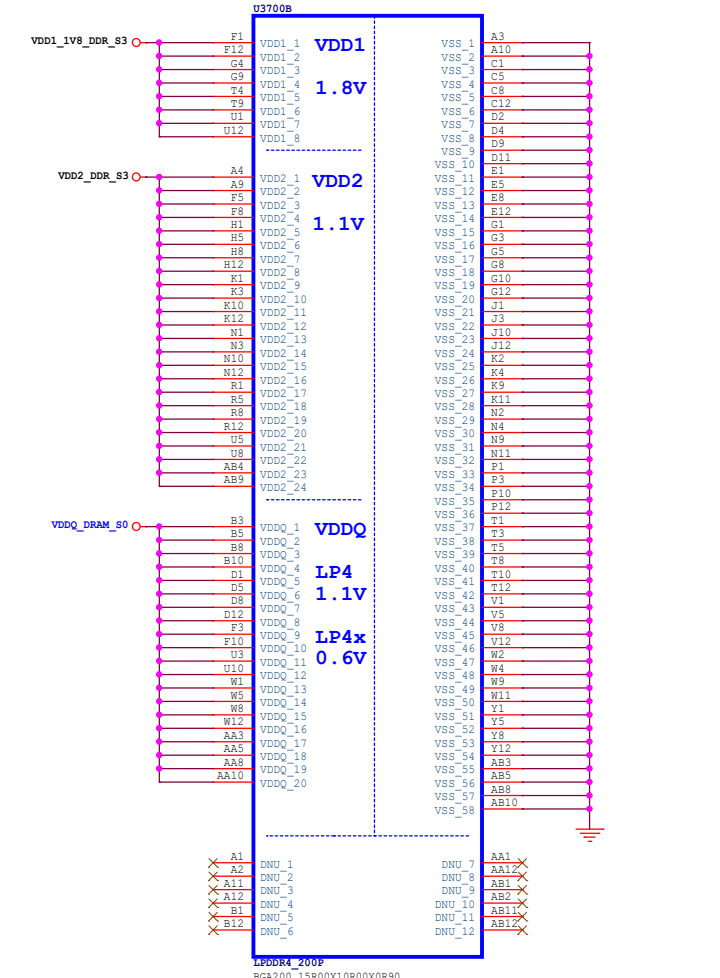
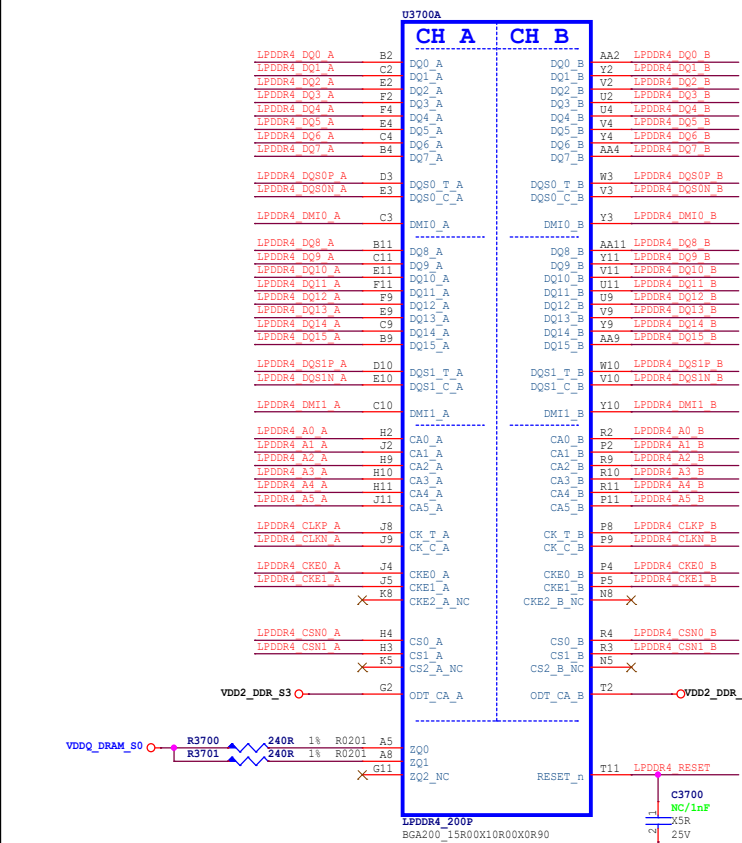


ShenZhen HugSun Technology Co., Ltd			
Project:	RP08B_RK3572		
File:	34.TF Card		
Date:	Friday, August 14, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	34 of 42

CODEC



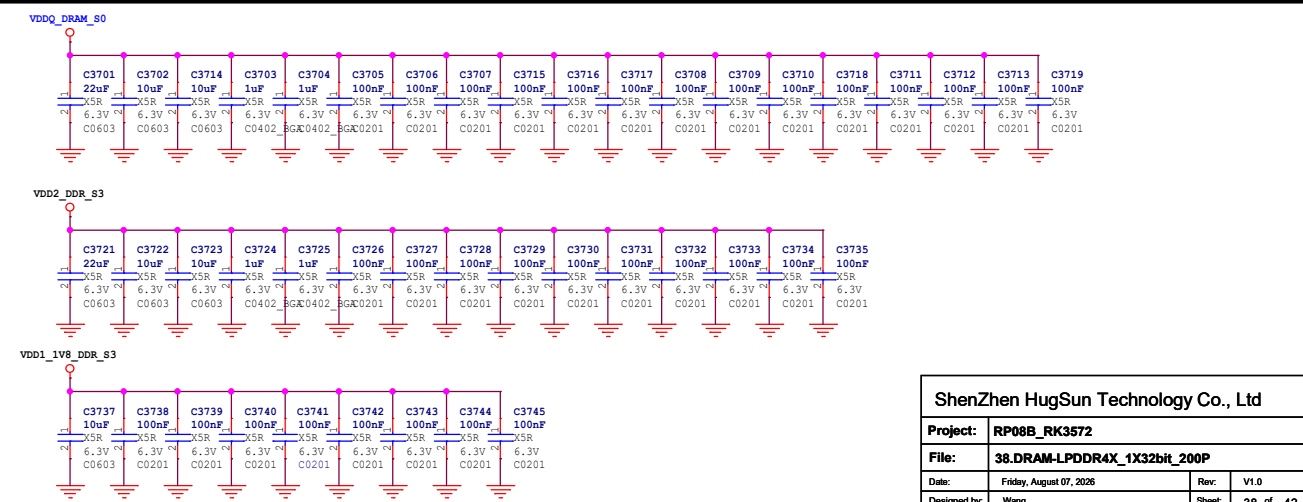
LPDDR4/4X (200BALL)

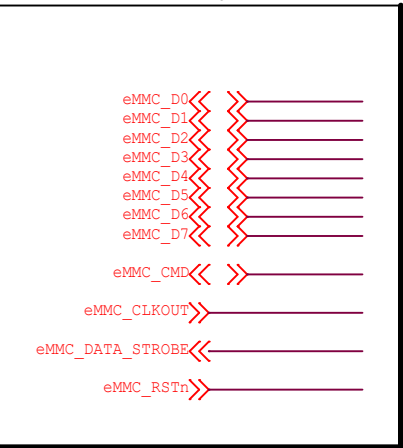


Note:

Sequence: VDD1-VDD2-VDDQ

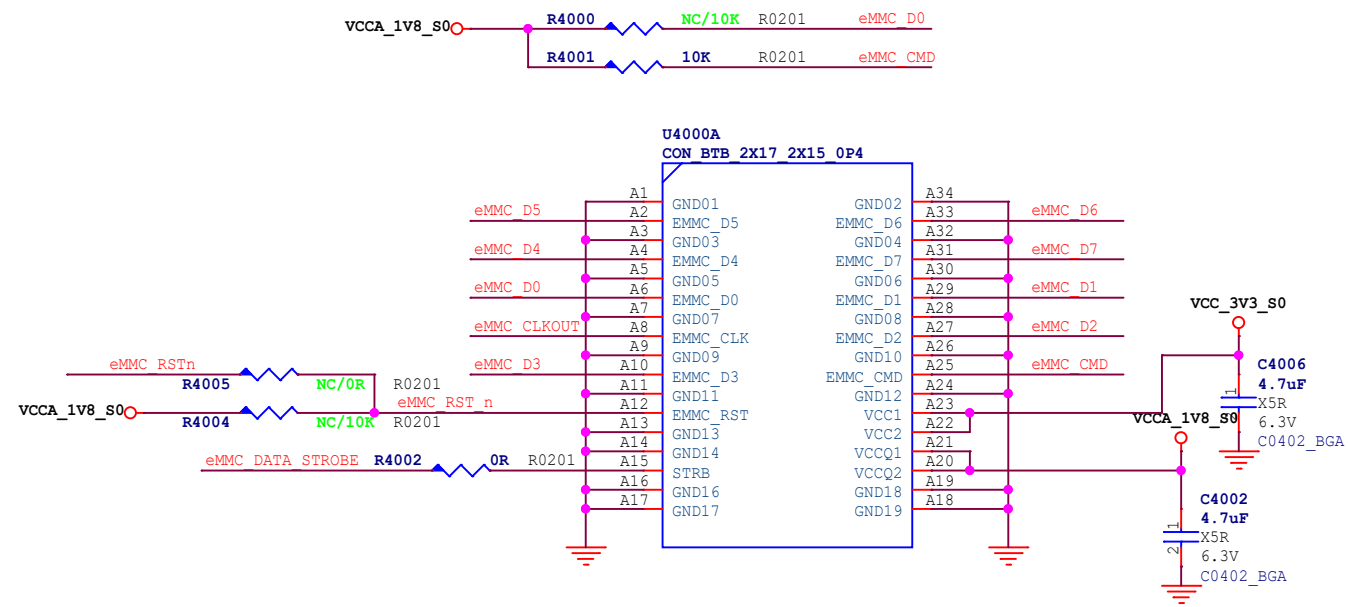
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65





4

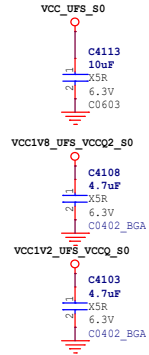
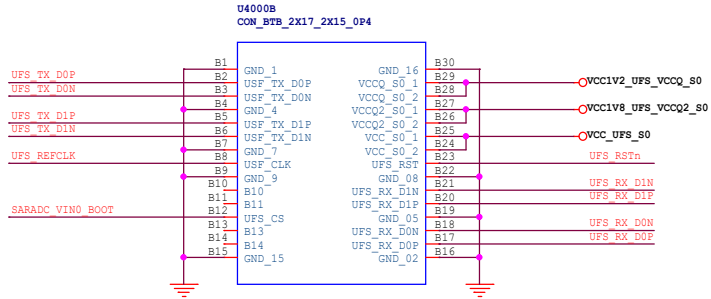
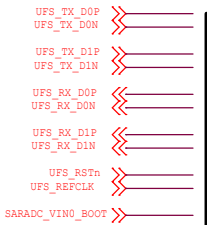
eMMC FLASH



ShenZhen HugSun Technology Co., Ltd

Project:	RP08B_RK3572		
File:	40.Flash-eMMC		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	40 of 42

UFS Flash



UFS POWER

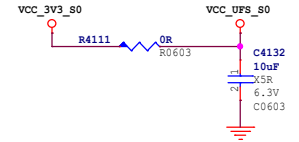
VCC: Supply voltage for the NAND memory device.
VCCQ/VCCQ2: Supply voltage used for the M-PHY interface and the memory controller.

Peak Values: Icc<600mA;
Iccq/Iccq2<800mA for 256GB

Supported Particles	VCCQ	VCCQ2	VCC	Default UFS device: UFS2.2
UFS2.0	1.2V	1.8V	3.3V	
UFS2.1	No Connect	1.8V	3.3V	
UFS2.2	No Connect	1.8V	3.3V	
UFS3.0	1.2V	No Connect	2.5V/3.3V	Do not support UFS4.0 Device!
UFS3.1	1.2V	No Connect	2.5V/3.3V	

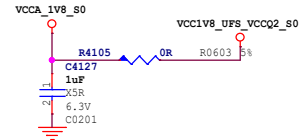
Note:
Sequence: VDDA_1V2_S0->VCCQ2 or VCCQ
VDDA_1V2_S0 is the power of REF CK & RST N in RK SOC, which needs to be powered on before UFS particles

VCC

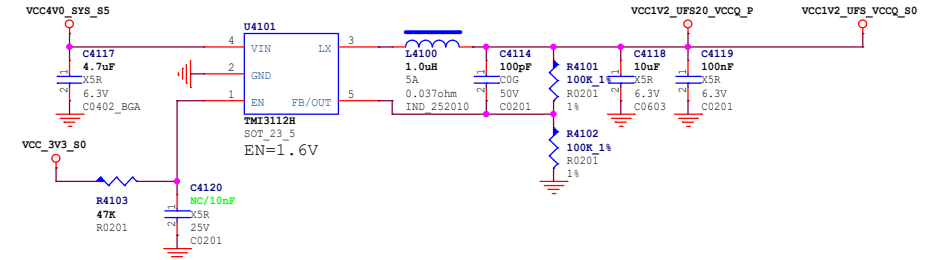


Please select the voltage according to different UFS manufactures.

VCCQ or VCCQ2



VCCQ(For UFS2.0 only)

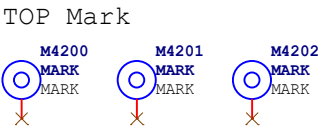


Note:
Power for UFS 2.0 devices only!!!
If UFS 2.0 devices aren't needed, remove this circuit to save cost.
For particles that require VCCQ and VCCQ2, the following timing needs to be met:
Sequence: VDDA_1V2_S0->VCCQ2->VCCQ

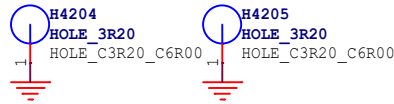
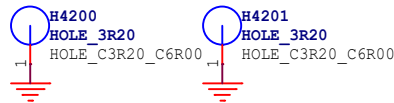
ShenZhen HugSun Technology Co., Ltd			
Project:	RP08B_RK3572		
File:	41.UFS		
Date:	Friday, August 07, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	41 of 42

Heatsink

Mark



Hole



ShenZhen HugSun Technology Co., Ltd			
Project:	RP08B_RK3572		
File:	42.Mark/Hole/Heatsink		
Date:	Thursday, August 13, 2026	Rev:	V1.0
Designed by:	Wang	Sheet:	42 of 42